SNES uPD6376 Pinout by [Jonathon W. Donaldson (jwdonal)](#) (special thanks to [Martin Korth (nocash)](#))

Designator	Name	Desc	SOIC16N_M	Type	Owner	Show	Number	Name
1	FSSEL	When this pin is low/open, L-ch data and R-ch data is input in time-division from Pin 15. When this pin is High, L-ch data is input from Pin 15, and R-ch data is input from Pin 14. (Pulled down in IC with 100-kO resistor) (GND)	1	Input	1	True	True	FSSEL
2	DGND	Digital ground	2	Power	1	True	True	DGND
3	NC		3	Passive	1	True	True	NC
4	DVDD	Digital power	4	Power	1	True	True	DVDD
5	AGND	Analog ground (NC)	5	Power	1	True	True	AGND
6	ROUT	Right analog signal output pin (to LM324)	6	Output	1	True	True	ROUT
7	AVDD	Analog power	7	Power	1	True	True	AVDD
8	AVDD	Analog power	8	Power	1	True	True	AVDD
9	RREF	Reference voltage pin. Normally connected to AGND through capacitor to lower impedance. (GND)	9	Passive	1	True	True	RREF
10	LREF	Reference voltage pin. Normally connected to AGND through capacitor to lower impedance. (GND)	10	Passive	1	True	True	LREF
11	LOUT	Left analog signal output pin (to LM324)	11	Output	1	True	True	LOUT
12	AGND	Analog ground	12	Power	1	True	True	AGND
13	LRCK	When FSSEL is low/open: functions as L-R judgment signal. When FSSEL is high: functions as input data word judgment signal. (32000Hz) (from S-DSP)	13	Input	1	True	True	LRCK
14	LRSEL	When FSSEL is low/open: functions as pin to select L-R polarity for LRCK. When LRCK is high, set LRSEL low to input L-ch data; When LRCK is low, set LRSEL high to input R-ch. When FSSEL is high: functions as R-ch serial data input. (GND)	14	Input	1	True	True	LRSEL
15	SI	When FSSEL is low/open: functions as L-ch and R-ch serial data input alternately. When FSSEL is high: functions as L-ch serial data input. (from S-DSP)	15	Input	1	True	True	SI
16	CLK	Read clock for serial data (1.536MHz) (from S-DSP)	16	Input	1	True	True	CLK