SCHEMATIC REV	PB NUMBER	VER	BOM RELEASE DATE
K7	X803600-011	RETAIL	XX/XX/XX

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[3]	RESET/ENABLE DIAGRAM
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[5]	CPU, FSB
[6]	CPU, FSB POWER + PLL POWER
[7]	CPU, CORE POWER
[8]	CPU, POWER
[9]	CPU, DECOUPLING
[10]	CPU, DECOUPLING
[11]	CPU, DECOUPLING
[12]	GPU, FSB
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[14]	GPU, MEMORY CONTROLLER A + B
[15]	GPU, MEMORY CONTROLLER C + D
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[17]	GPU, CORE POWER + MEM POWER
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[22]	MEMORY, B (TOP)
[23]	MEMORY, B MIRRORED (BOTTOM)
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[25]	MEMORY, C MIRRORED (BOTTOM)
[26]	MEMORY, D (TOP)
[27]	MEMORY, D MIRRORED (BOTTOM)
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[32]	POWER TRACE EMI CAPS

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[37]	SB, STANDBY POWER + DECOUPLE
[38]	SB, MAIN POWER + DECOUPLE
[39]	SB OUT, ETHERNET
[40]	SB OUT, AUDIO
[41]	SB OUT, FLASH
[42]	SB OUT, FAN + INFRARED + BUTTONS
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[45]	CONN, GAME PORTS + MEMORY PORTS
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[52]	VREGS, GPU CONTROLLER
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[54]	VREGS, SWITCHED 1.8, 5.0V
[55]	VREGS, LINEAR REGULATORS
[56]	XDK, DEBUG CONN
[57]	DEBUG BOARD, CPU + GPU BREAKOUT
[58]	DEBUG BOARD, CPU CONN
[59]	DEBUG BOARD, CPU CONN + TERM
[60]	DEBUG BOARD, CPU TERM
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[62]	DEBUG BOARD, GPU CONN + TERM
[63]	XDK, LEDS
[64]	LABELS AND MOUNTING

XENON
RETAIL
REV K7
FAB K

RULES: (APPLIED WHEN POSSIBLE)

1.) MSB TO LSB IS TOP TO BOTTOM
2.) WHEN POSSIBLE: INPUTS ON LEFT, OUTPUTS ON RIGHT
3.) ORDER OF PAGES=CHIP INTERFACES, TERMINATION, POWER, DECOUPLING
4.) AVOID USING OFF PAGE CONNECTORS FOR ON PAGE CONNECTIONS
5.) LANED SIGNALS ARE GROUPED ON SYMBOLS
6.) TRANSIMITTER NAME USED AS PREFIX WITH RX AND TX CONNECTIONS
7.) SUFFIX V IS USED FOR VOLTAGE RAIL SIGNAL NAMES
8.) SUFFIX _DP AND _DN ARE USED FOR DIFFERIENTAL PAIRS
9.) UNNAMED NETS ARE NAMED WITH /2 TEXT SIZE
10.) SUFFIX _N FOR ACTIVE LOW OR N JUNCTION
12.) SUFFIX _P FOR P JUNCTION
13.) SUFFIX _EN FOR ENABLE
14.) 'CLK' FOR CLOCKS, 'RST' FOR RESETS
15.) PWRGD FOR POWER GOOD

[PAGE_TITLE=COVER PAGE]

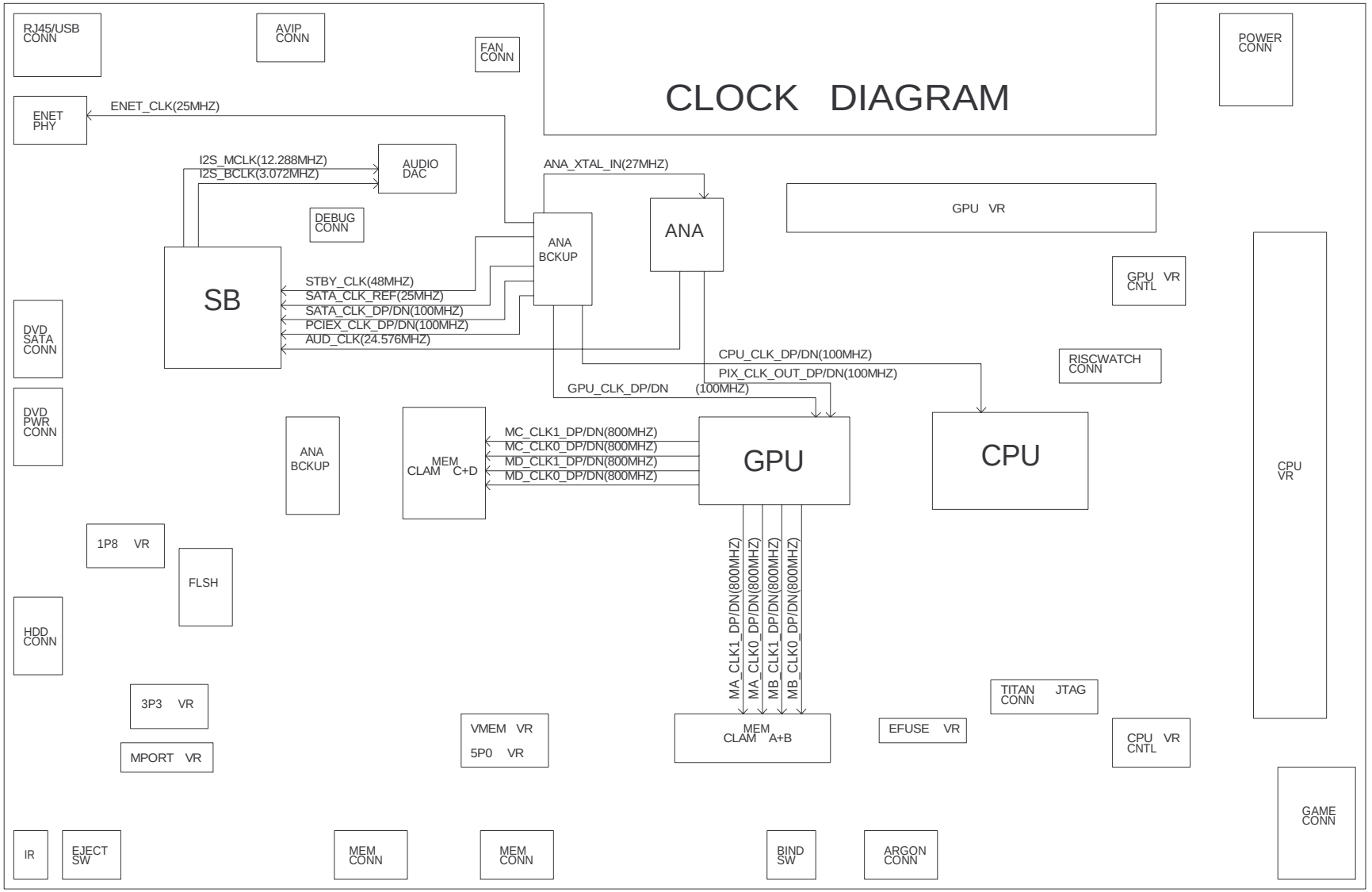
DRAWING
XENON_FABK
Wed Aug 24 09:41:55 2005

XENON

PLEASE REFER TO THE XENON DESIGN SPEC

BOM RELEASE DATE	XX/XX/XX	PB NUMBER X803600-011		
SIGNATURE	DATE	MICROSOFT XBOX		
DRN BY		TITLE SCH, PBA, XENON		
CHK BY				
ENGR APVD				
APVD				
APVD				
MICROSOFT CONFIDENTIAL		PROJECT NAME XENON_RETAIL	PAGE 1/73	REV K7

CLOCK DIAGRAM



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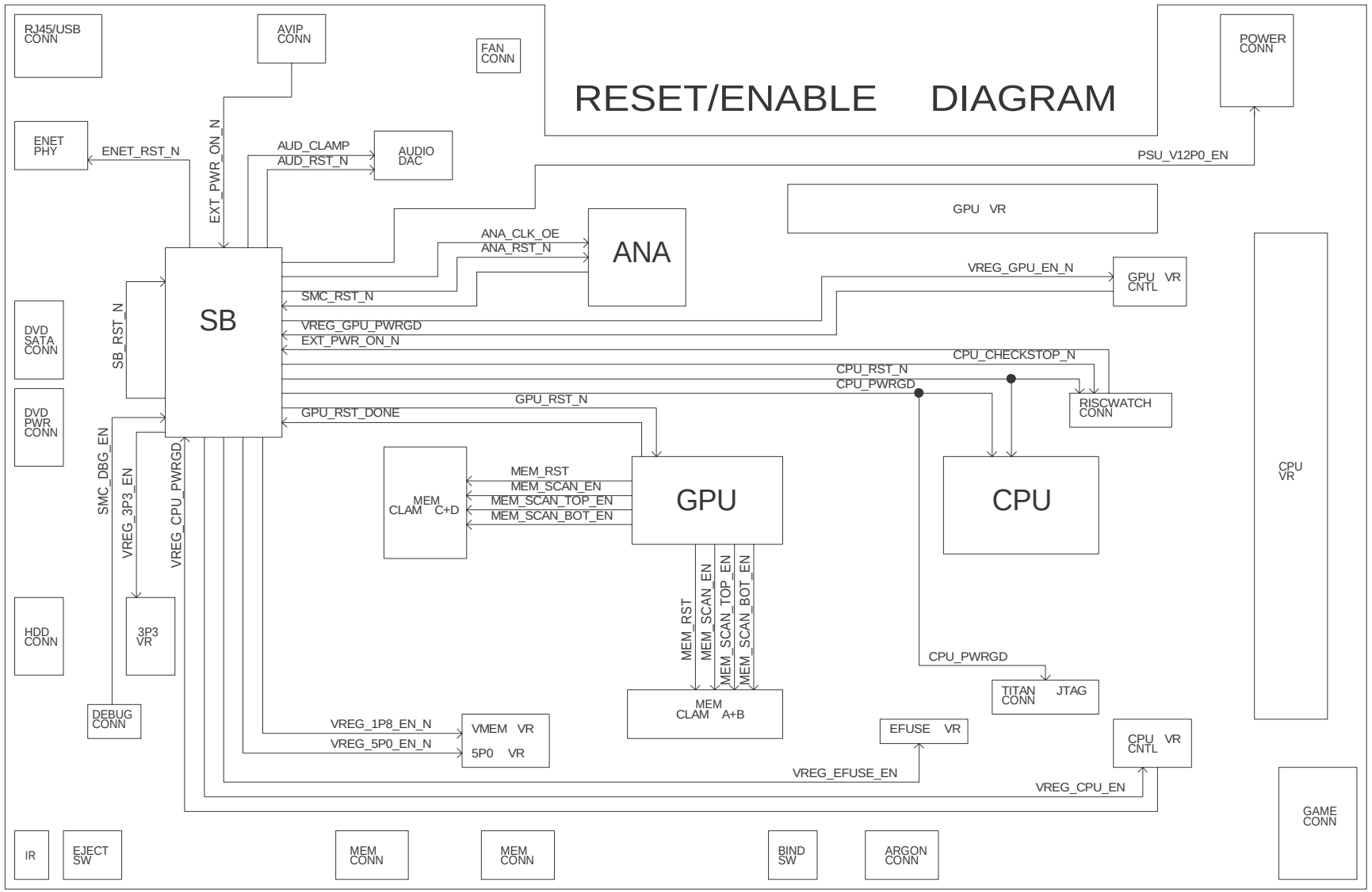
DRAWING
XENON_FABK
Wed Jul 27 21:53:30 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	2/73	K7



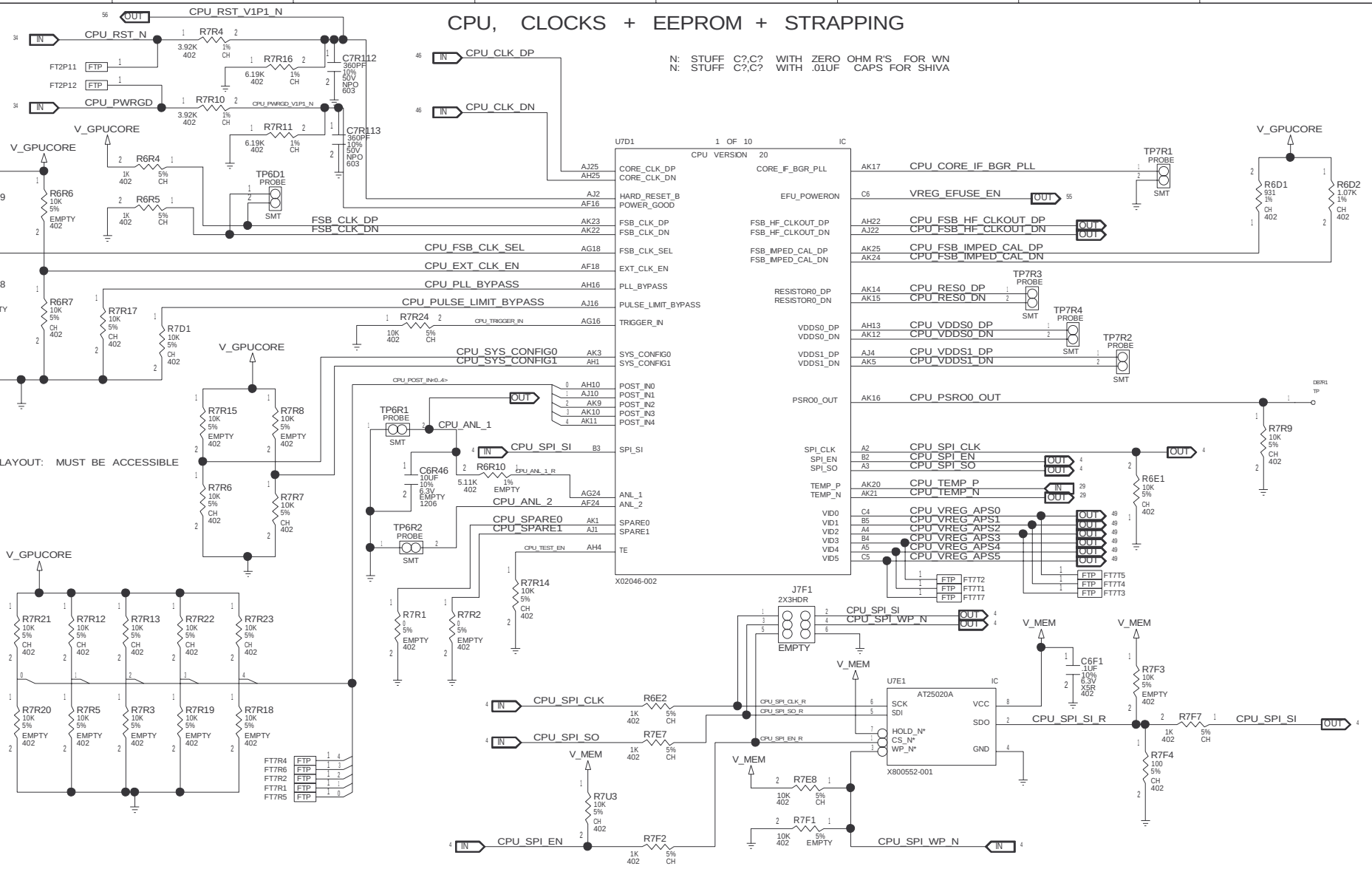
[PAGE_TITLE=RESET/ENABLE DIAGRAM]

DRAWING
XENON_FABK
Wed Jul 27 21:53:44 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	3/73	K7

CPU, CLOCKS + EEPROM + STRAPPING

N: STUFF C?,C? WITH ZERO OHM R'S FOR WN
N: STUFF C?,C? WITH .01UF CAPS FOR SHIVA

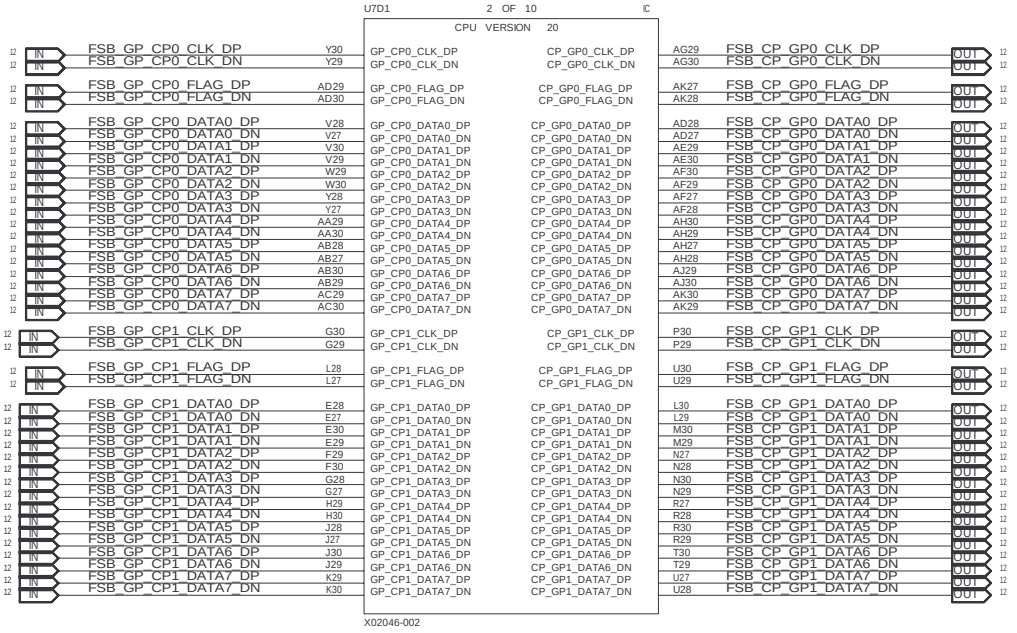


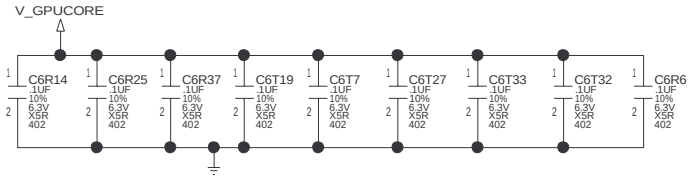
[PAGE_TITLE=CPU, CLOCKS + EEPROM + STRAPPING]

DRAWING
XENON_FABK
Wed Aug 24 09:27:00 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	4/73	K7

CPU, FSB



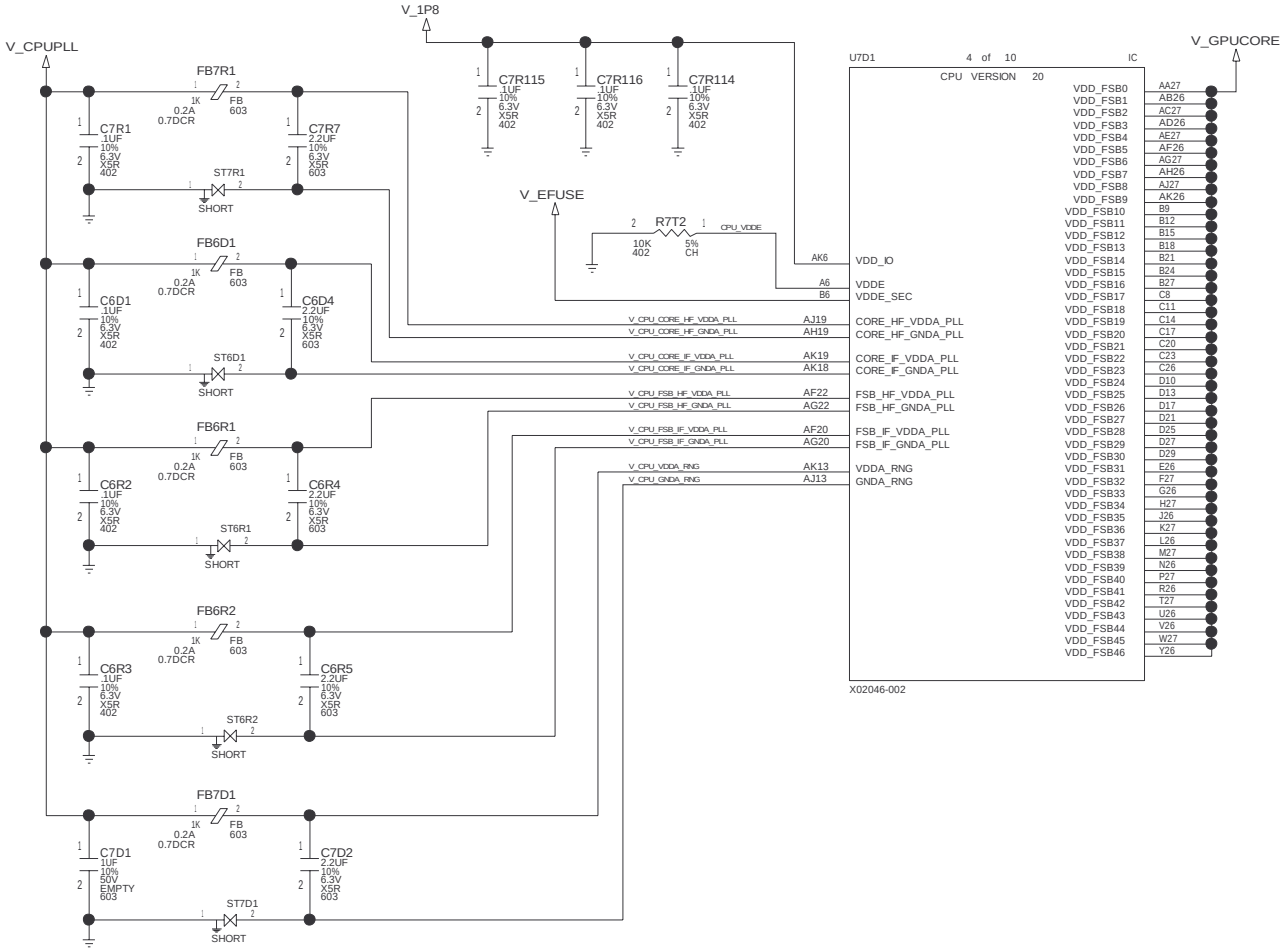


[PAGE_TITLE=CPU, FSB]

DRAWING
XENON_FABK
Wed Aug 24 09:27:01 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	5/73	K7

CPU, FSB POWER + PLL POWER

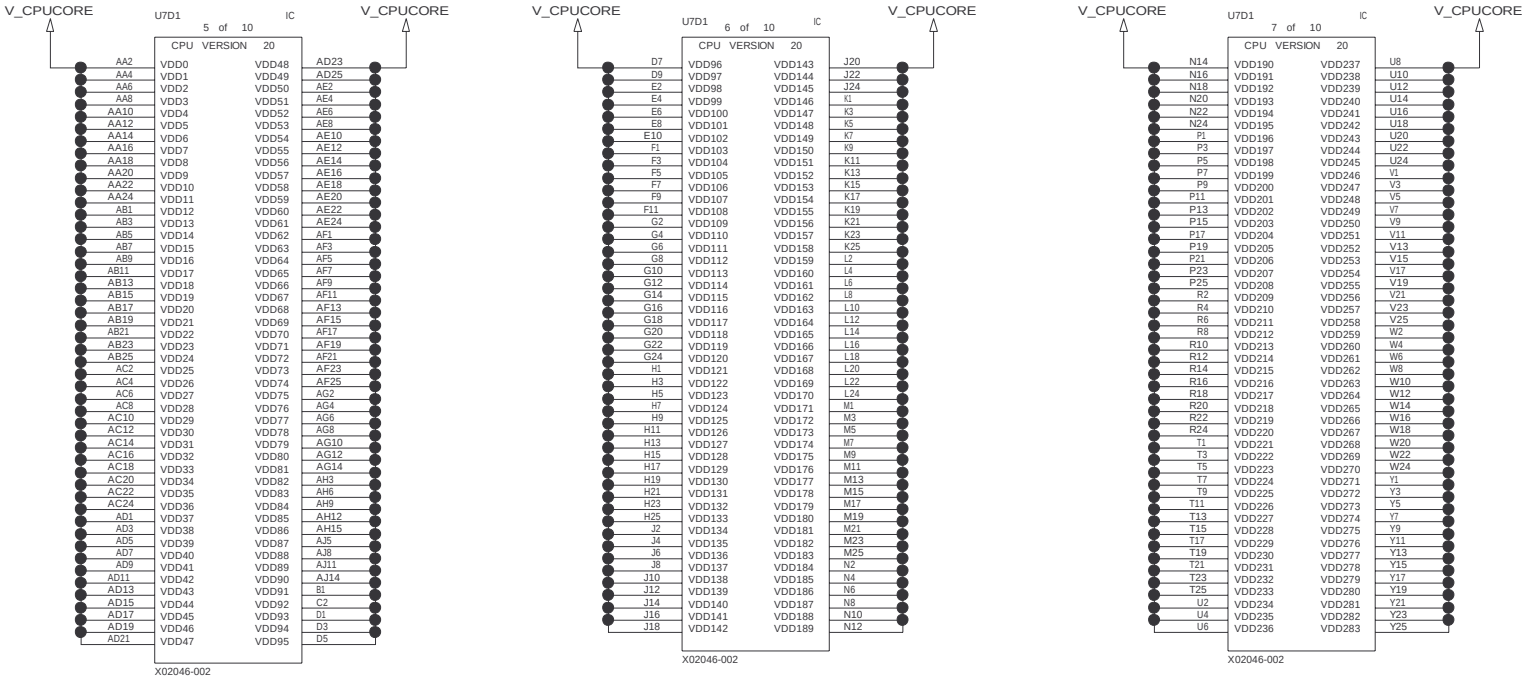


[PAGE_TITLE=CPU, FSB POWER + PLL POWER]

DRAWING
XENON_FABK
Wed Aug 24 09:27:01 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	6/73	K7

CPU, CORE POWER

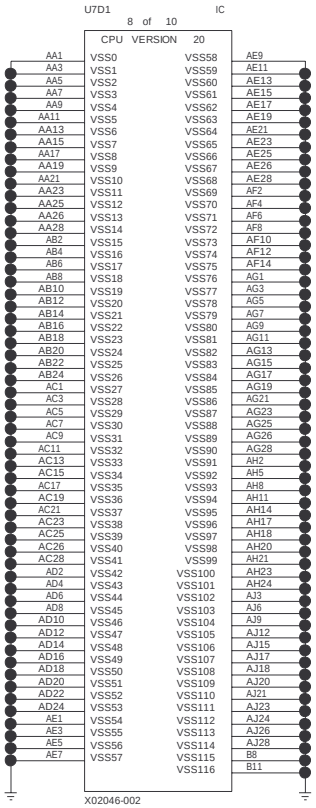


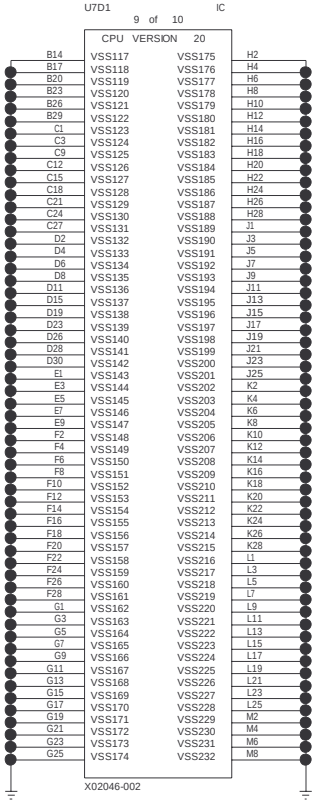
[PAGE_TITLE=CPU, CORE POWER]

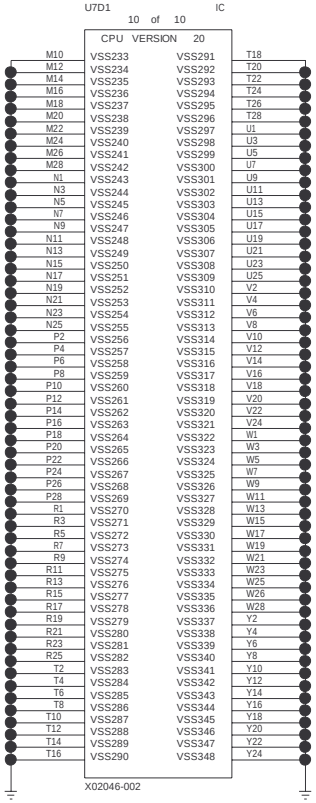
DRAWING
XENON_FABK
Wed Aug 24 09:27:01 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	7/73	K7

CPU, POWER





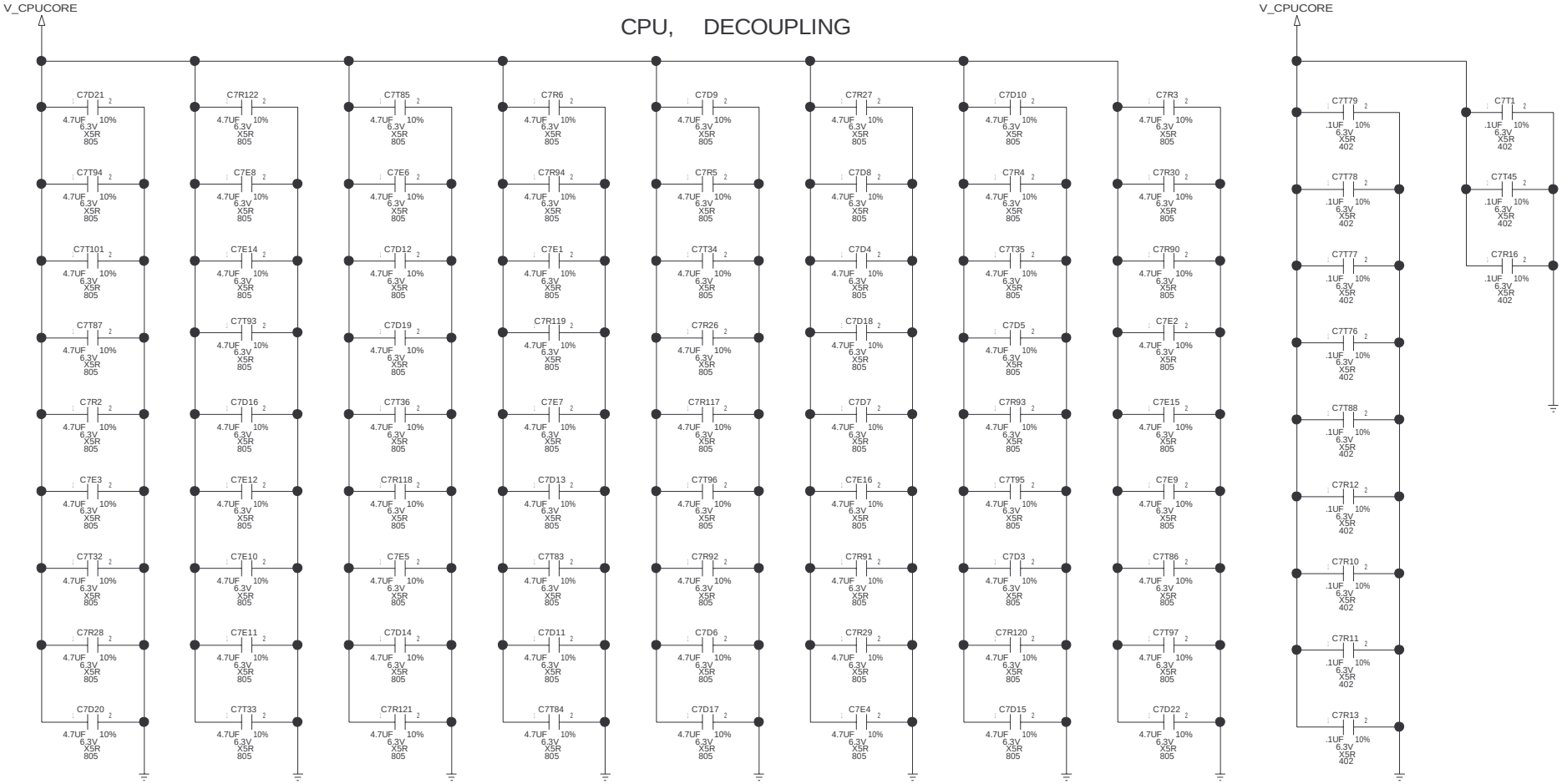


[PAGE_TITLE=CPU, POWER]

DRAWING
XENON_FABK
Wed Aug 24 09:27:02 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	8/73	K7

CPU, DECOUPLING



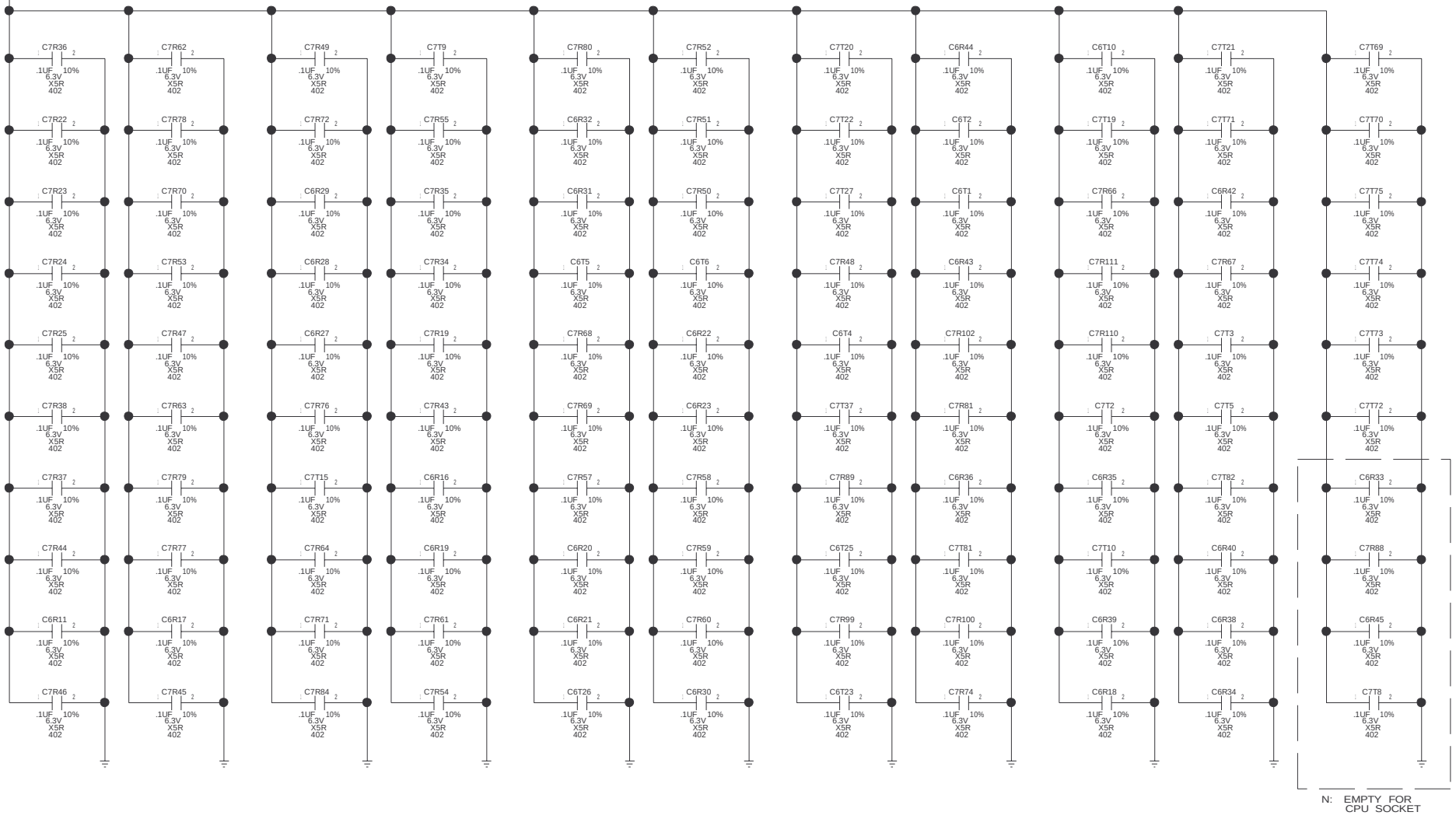
[PAGE_TITLE=CPU, DECOUPLING]

DRAWING
XENON_FABK
Wed Aug 24 09:27:03 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	9/73	K7

V_CPUCORE

CPU, DECOUPLING



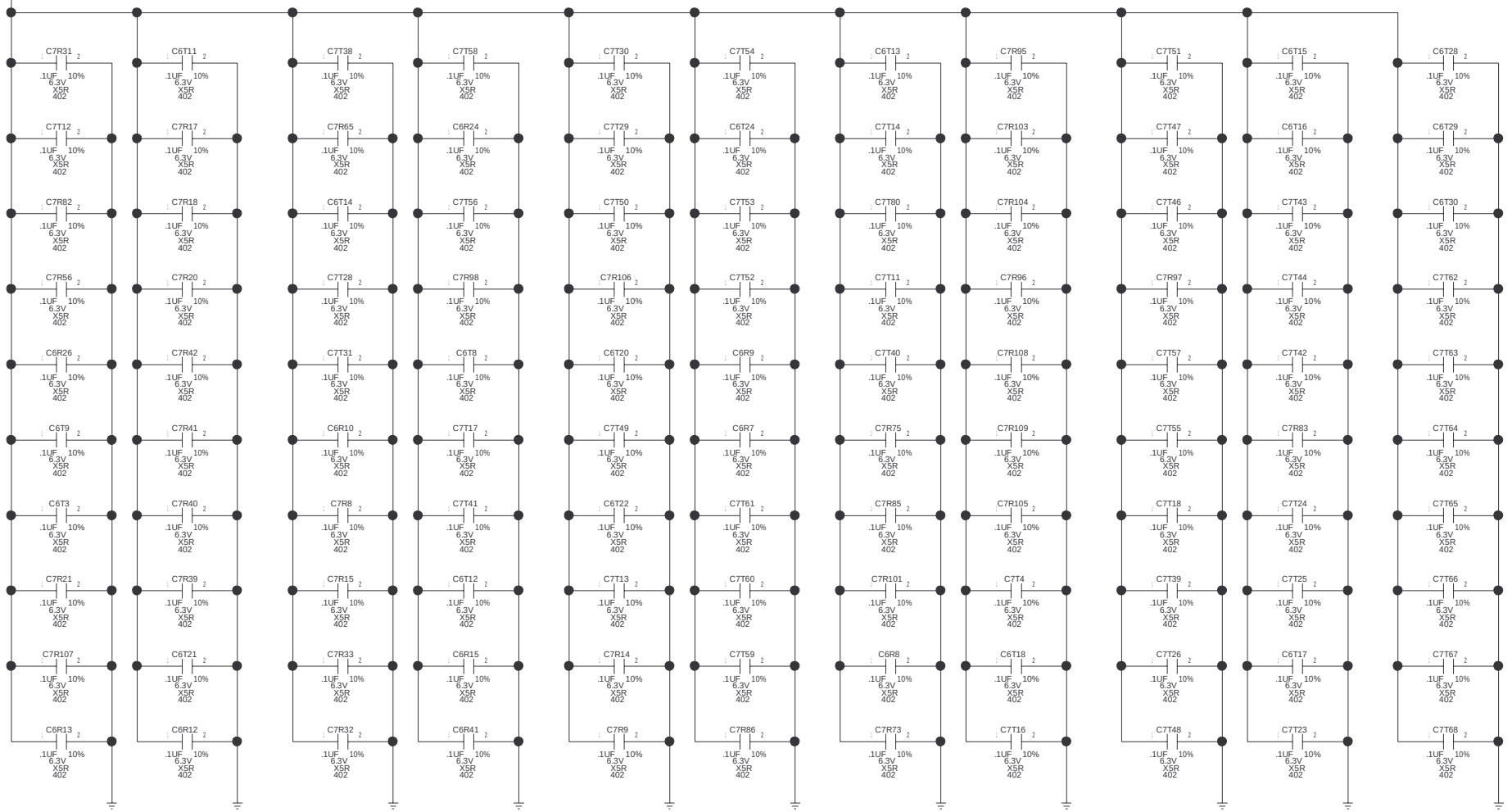
[PAGE_TITLE=CPU, DECOUPLING]

DRAWING
XENON_FABK
Wed Aug 24 09:27:03 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	10/73	K7

CPU, DECOUPLING

V_CPUCORE



[PAGE_TITLE=CPU, DECOUPLING]

DRAWING
XENON_FABK
Wed Aug 24 09:27:05 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
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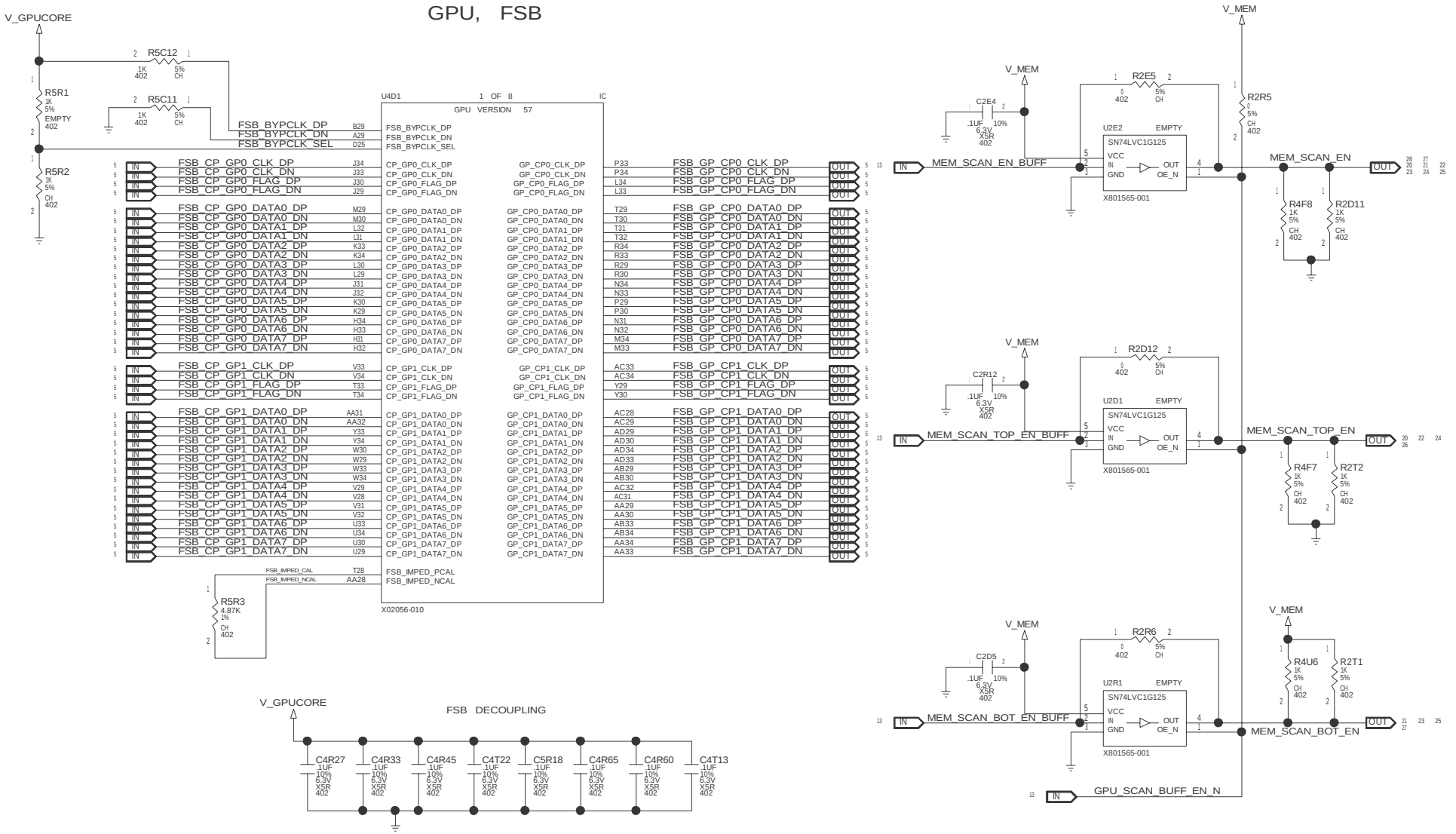
GPU, FSB



[PAGE_TITLE=GPU, FSB]

DRAWING
XENON_FABK
Wed Aug 24 09:27:06 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
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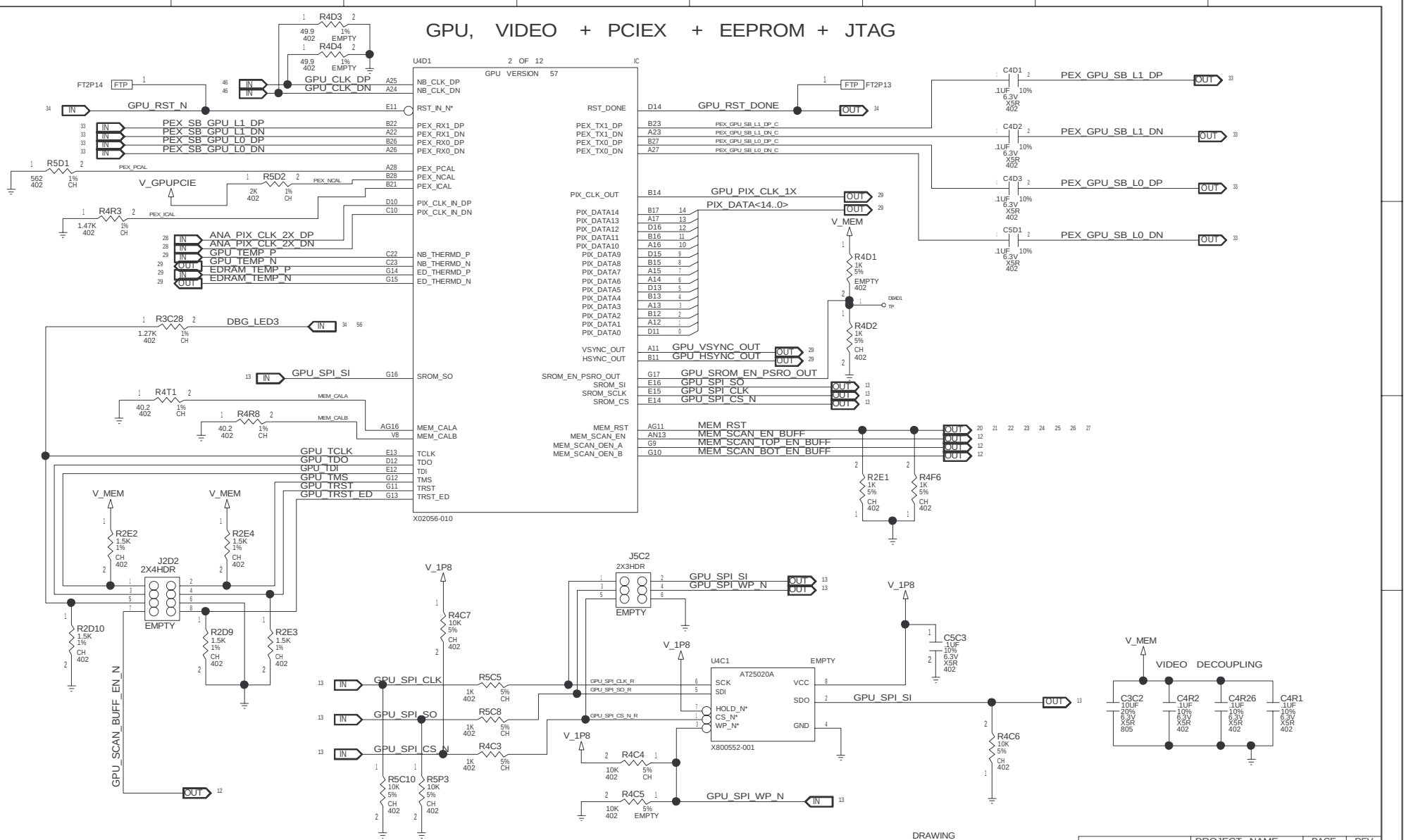
GPU, VIDEO + PCIEX + EEPROM + JTAG
U4D1
2 OF 12
GPU VERSION 57
GPU_CLK_DP
GPU_CLK_DN
GPU_RST_N
PEX_SB_GPU_L1_DP
PEX_SB_GPU_L1_DN
PEX_SB_GPU_L0_DP
PEX_SB_GPU_L0_DN
V_GPUPCIE
ANA_PIX_CLK_2X_DP
ANA_PIX_CLK_2X_DN
GPU_TEMP_P
GPU_TEMP_N
EDRAM_TEMP_P
EDRAM_TEMP_N
DBG_LED3
GPU_SPI_SI
MEM_CALA
MEM_CALB
GPU_TCLK
GPU_TDO
GPU_TDI
GPU_TMS
GPU_TRST
GPU_TRST_ED
GPU_RST_DONE
GPU_PIX_CLK_1X
PIX_DATA<14..0>
GPU_VSYNC_OUT
GPU_HSYNC_OUT
GPU_SROM_EN_PSRO_OUT
GPU_SPI_SO
GPU_SPI_CLK
GPU_SPI_CS_N
MEM_RST
MEM_SCAN_EN_BUFF
MEM_SCAN_TOP_EN_BUFF
MEM_SCAN_BOT_EN_BUFF
GPU_SPI_WP_N
PEX_GPU_SB_L1_DP
PEX_GPU_SB_L1_DN
PEX_GPU_SB_L0_DP
PEX_GPU_SB_L0_DN
V_MEM
V_1P8
VIDEO DECOUPLING
AT25020A
X800552-001
X02056-010
EMPTY
[PAGE_TITLE=GPU, VIDEO + PCIEX + EEPROM + JTAG]
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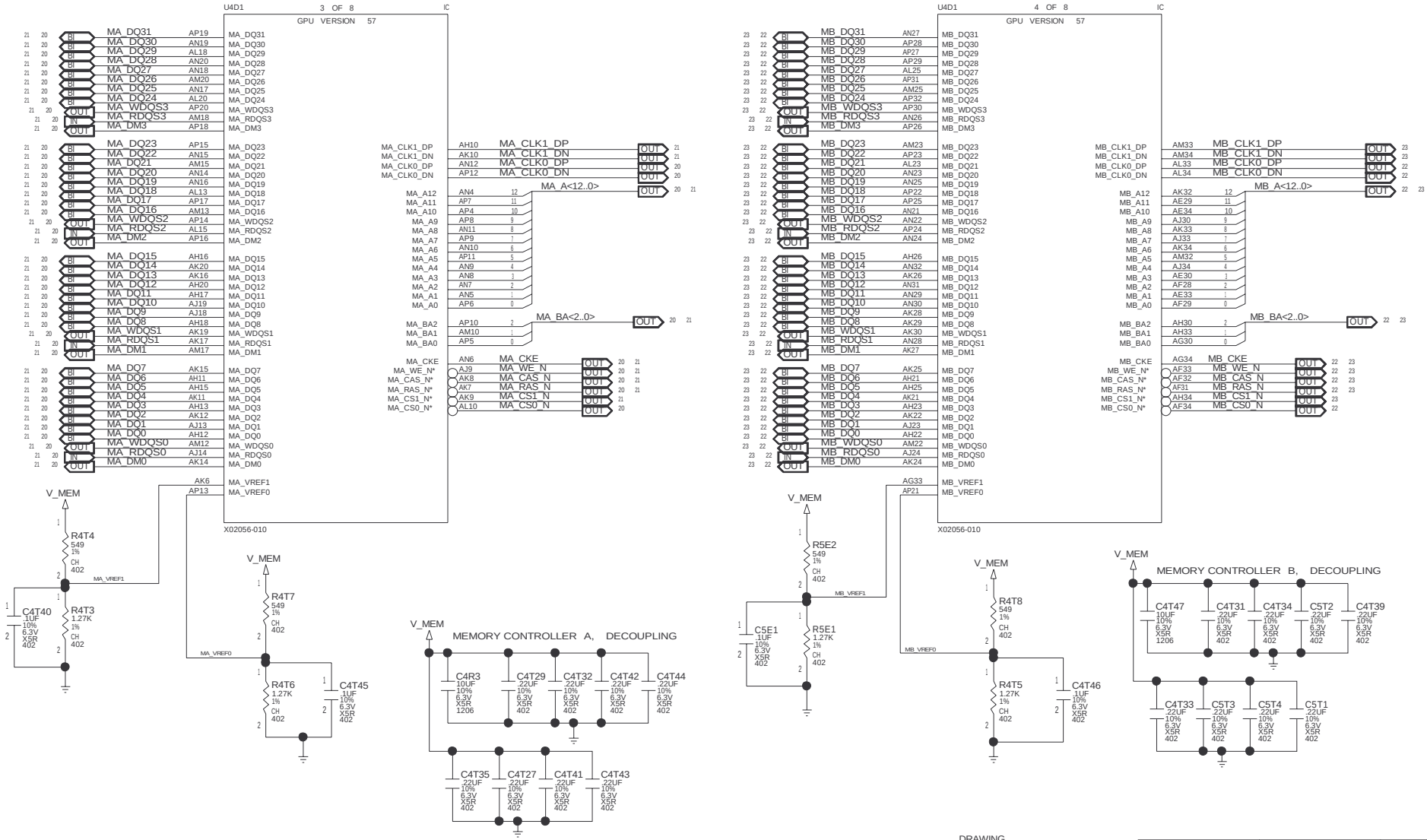
Wed Aug 24 09:27:07 2005
MICROSOFT CONFIDENTIAL
PROJECT NAME
XENON_RETAIL
PAGE
13/73
REV
K7

GPU, MEMORY CONTROLLER 0 PARTITION A & B



[PAGE_TITLE=GPU, MEMORY CONTROLLER A + B]

DRAWING
XENON_FABK
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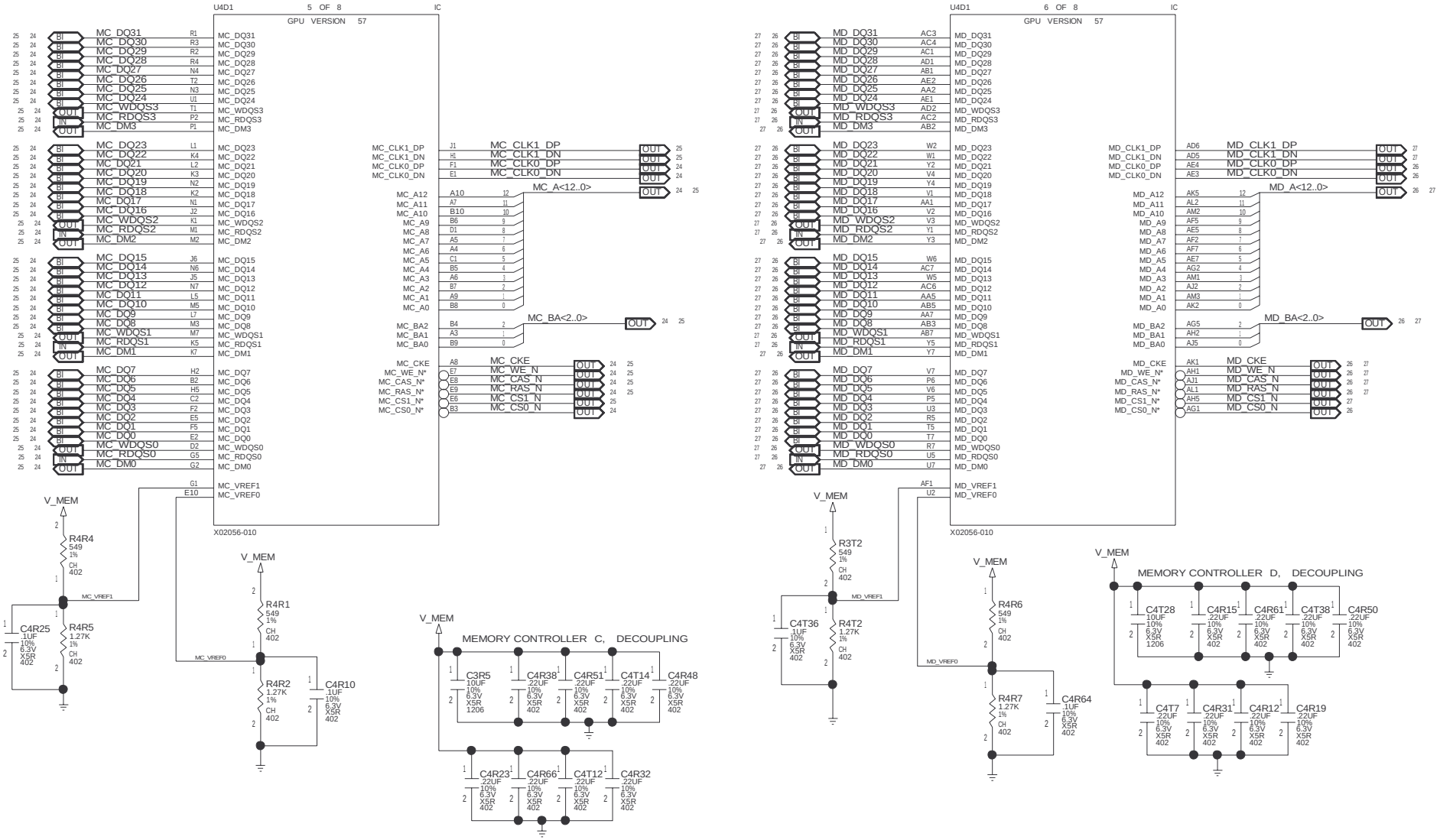
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	14/73	K7

GPU, MEMORY CONTROLLER 1 PARTITION C & D



PAGE_TITLE=[GPU, MEMORY CONTROLLER C + D]

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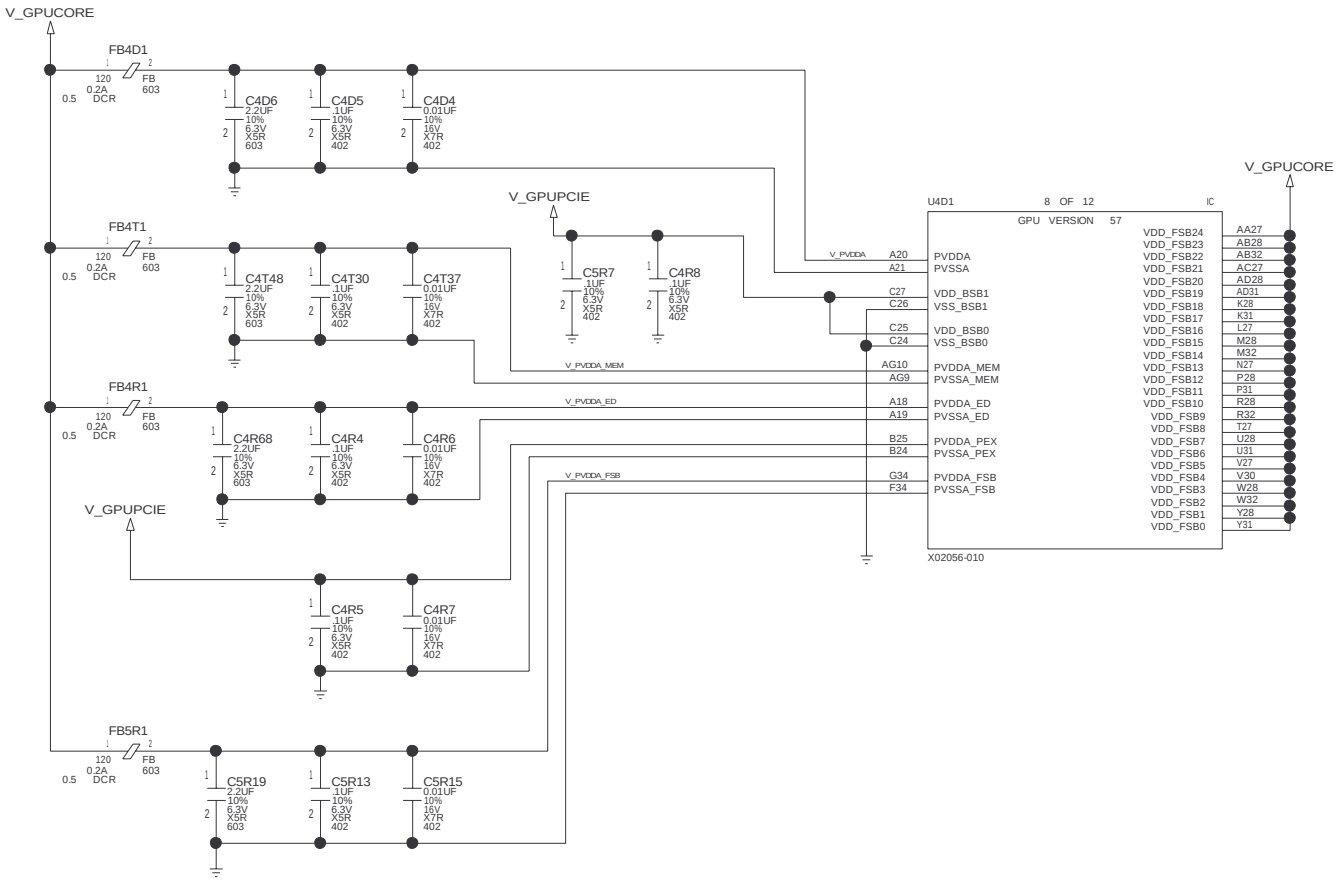
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	15/73	K7

GPU, PLL POWER + FSB POWER



[PAGE_TITLE=GPU, PLL POWER + FSB POWER]

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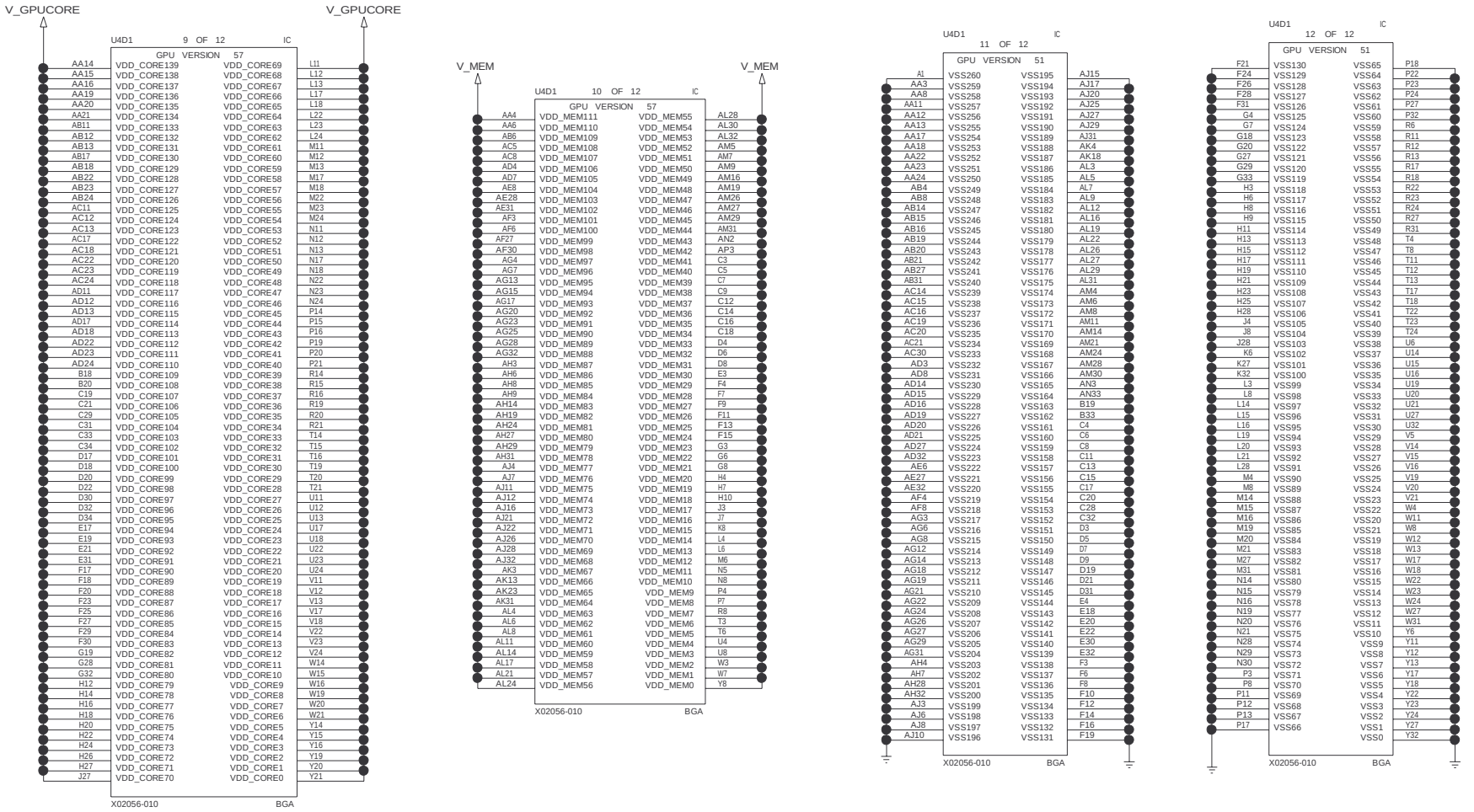
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	16/73	K7

GPU, CORE POWER + MEM POWER



[PAGE_TITLE=GPU, CORE POWER + MEM POWER]

DRAWING
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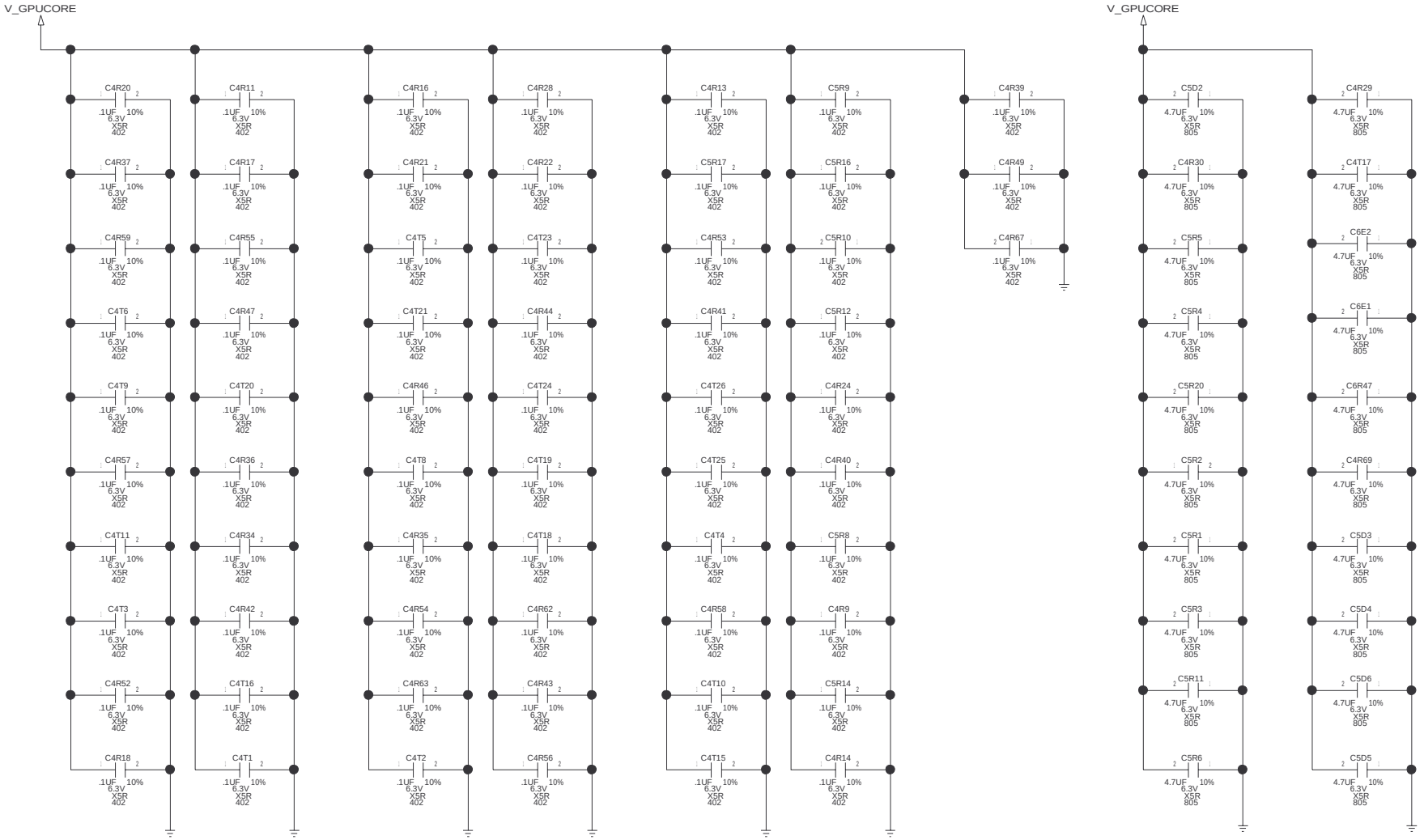
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	17/73	K7

GPU, DECOUPLING



[PAGE_TITLE=GPU, DECOUPLING]

DRAWING
XENON_FABK
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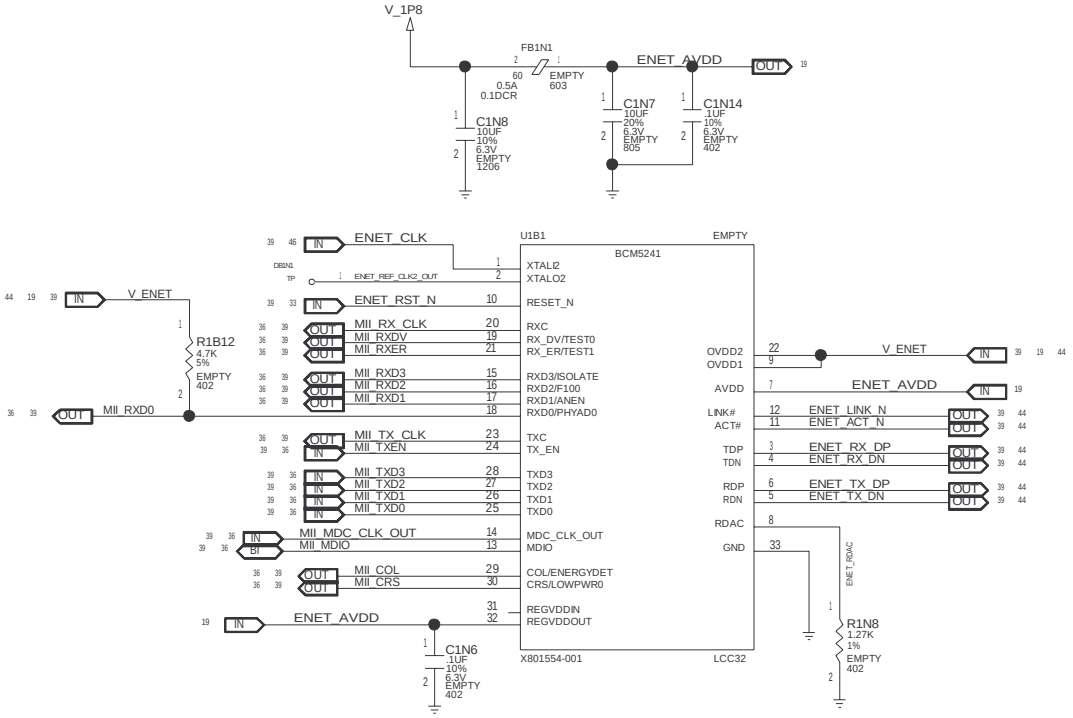
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	18/73	K7



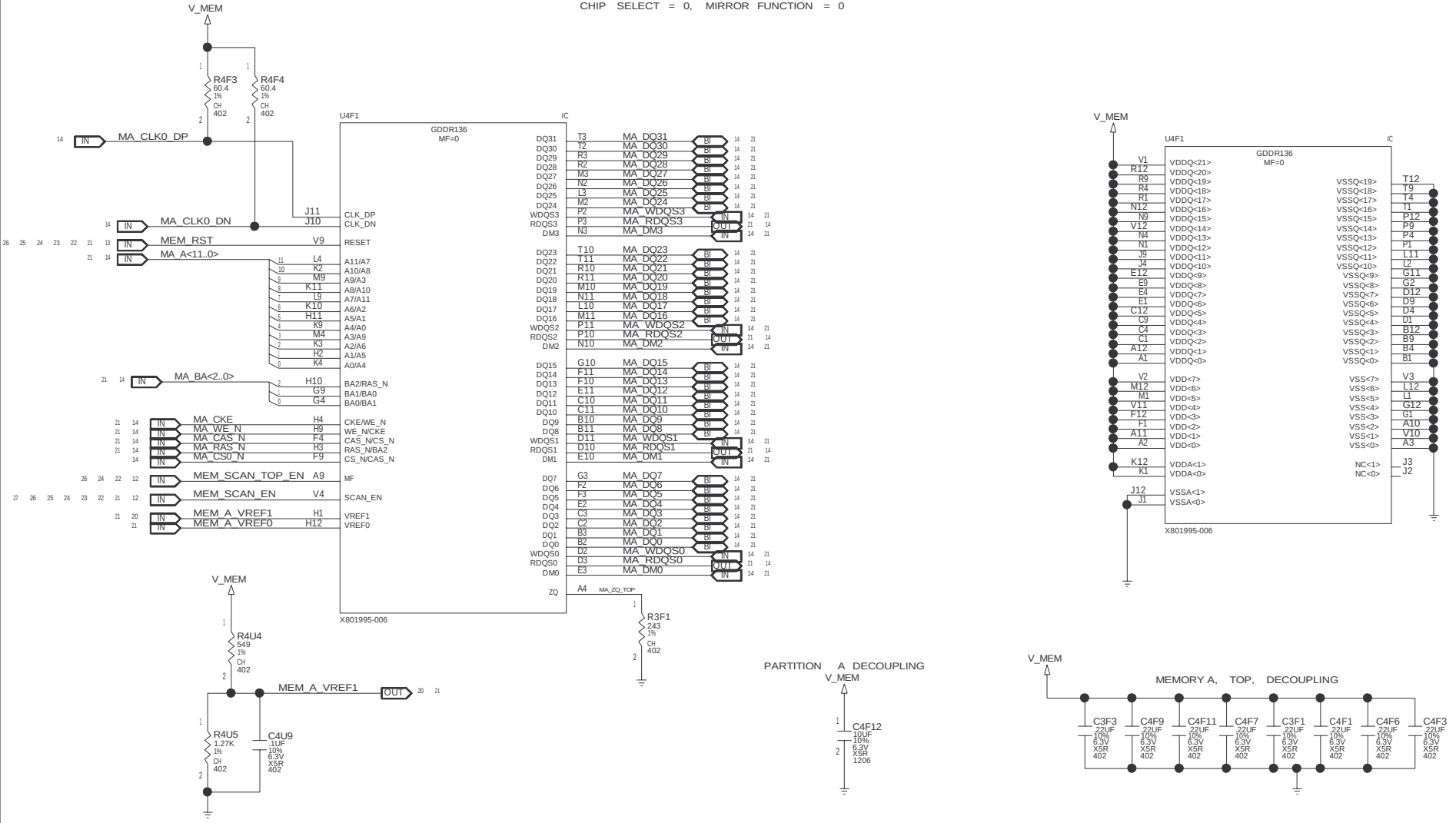
[PAGE_TITLE=DUAL ETHERNET PHY]

DRAWING
XENON_FABK
Wed Aug 24 09:27:13 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	19/73	K7

MEMORY PARTITION A, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0

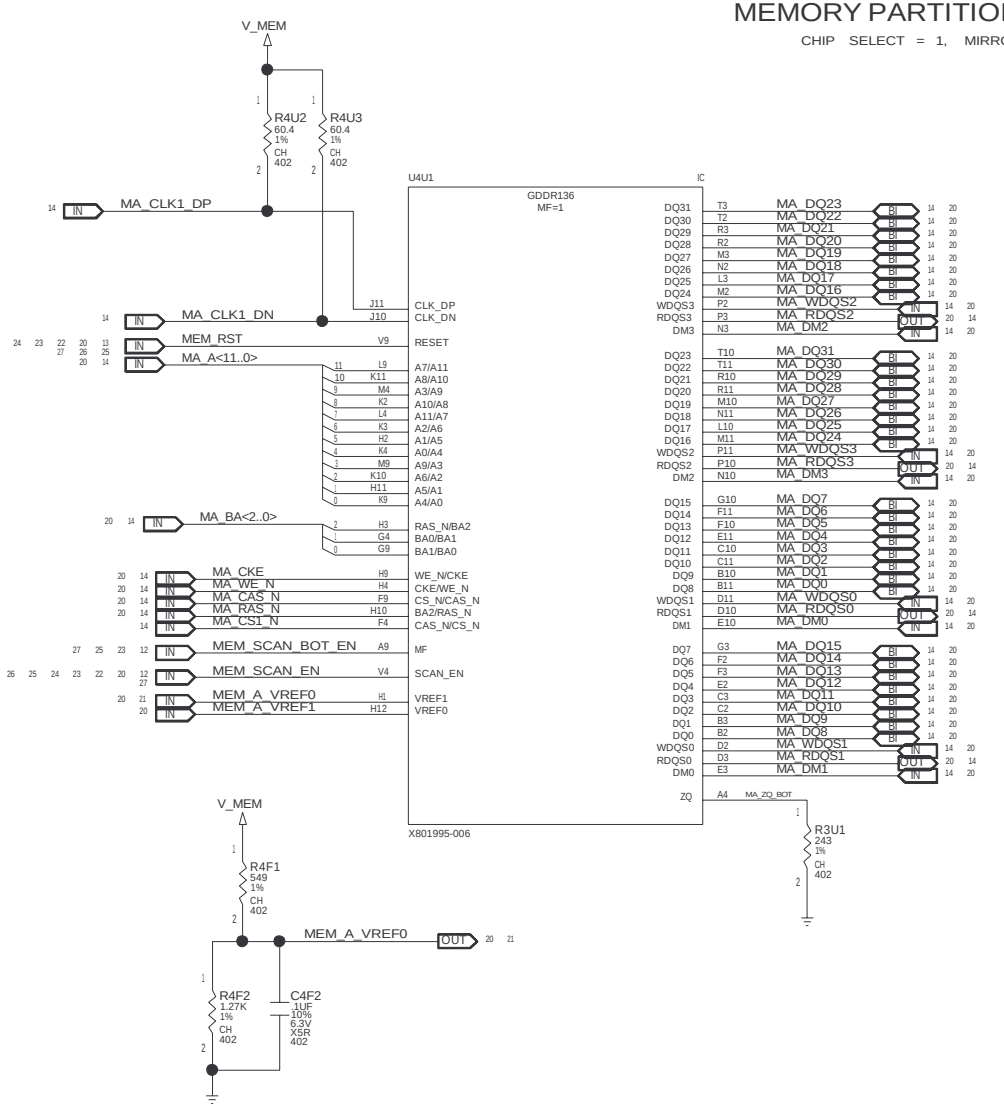


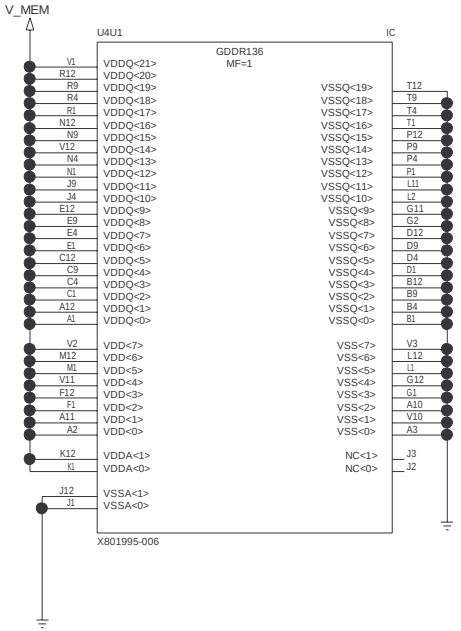
[PAGE_TITLE=MEMORY PARTITION A, TOP]

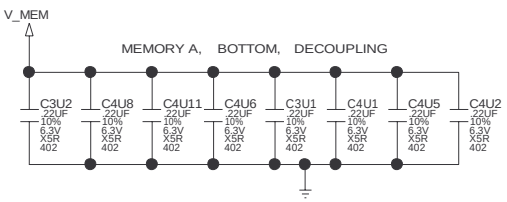
DRAWING							
XENON_FABK					MICROSOFT	PROJECT NAME	PAGE	REV
Wed Aug 24	09:27:13	2005			CONFIDENTIAL	XENON_RETAIL	20/73	K7

MEMORY PARTITION A, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1







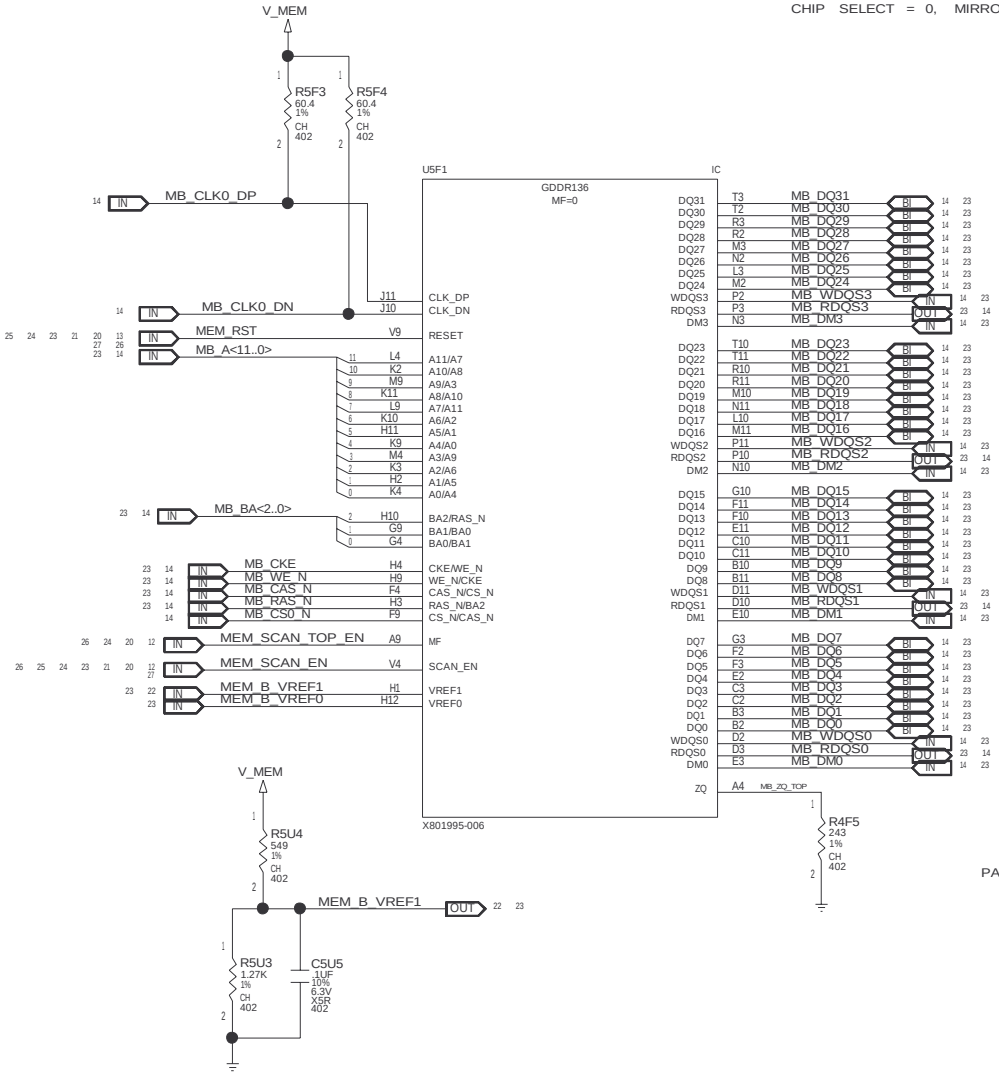
[PAGE_TITLE=MEMORY PARITION A, BOTTOM]

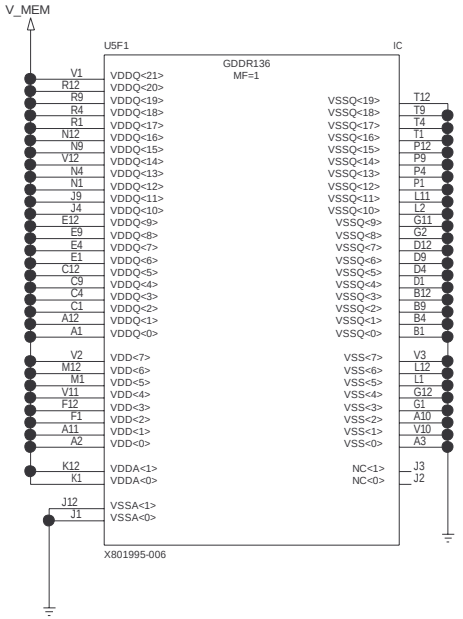
DRAWING
XENON_FABK
Wed Aug 24 09:27:14 2005

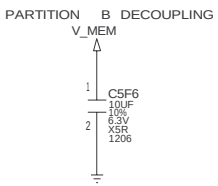
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	21/73	K7

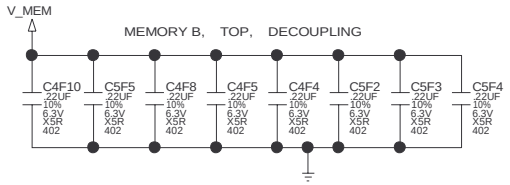
MEMORY PARTITION B, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0









[PAGE_TITLE=MEMORY PARITION B, TOP]

DRAWING
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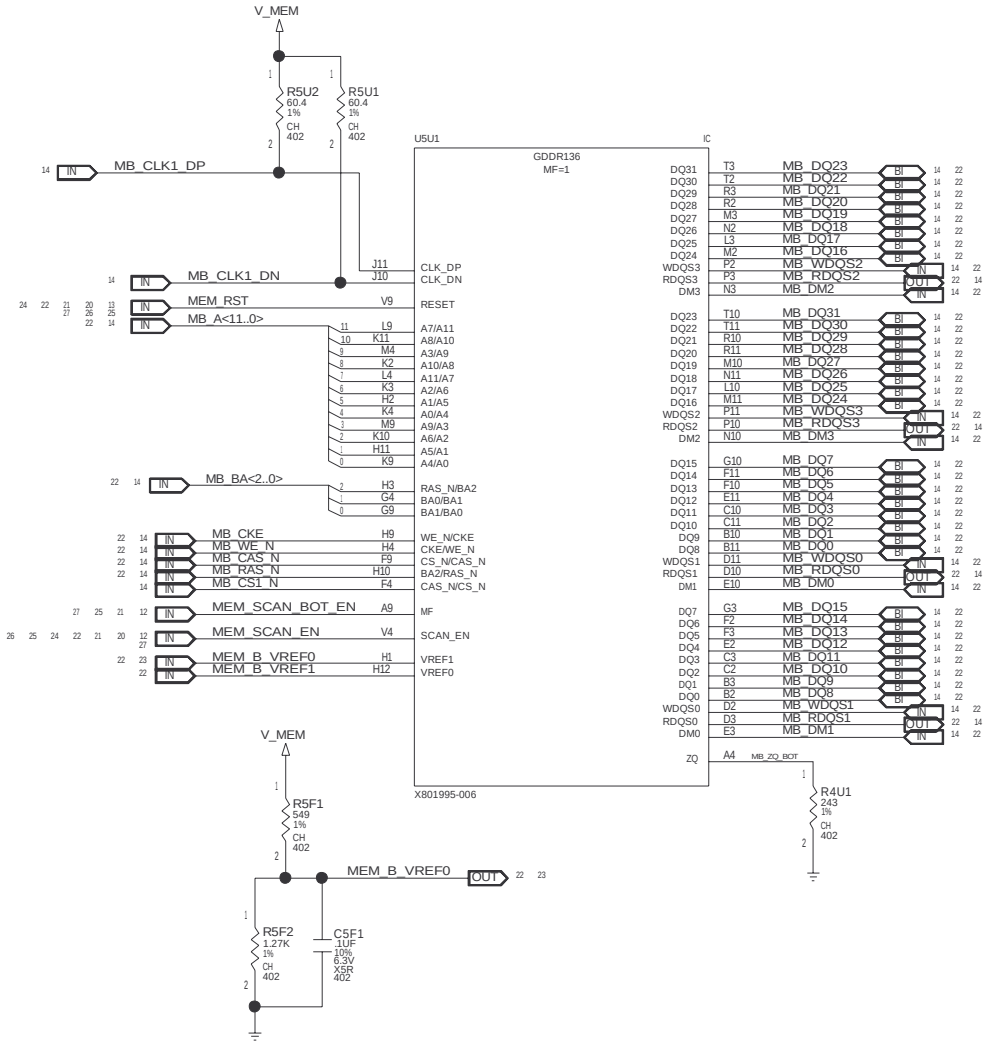
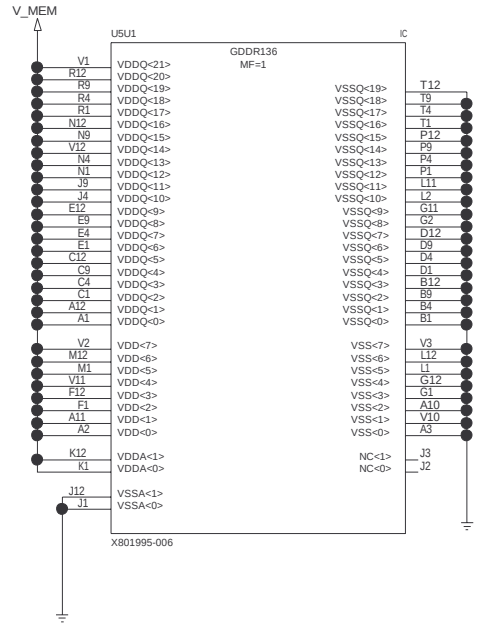
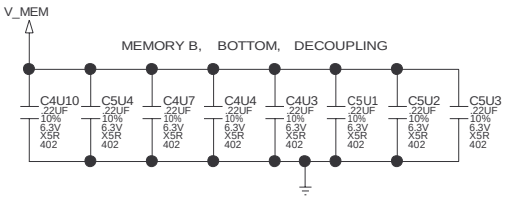
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	22/73	K7

MEMORY PARTITION B, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1







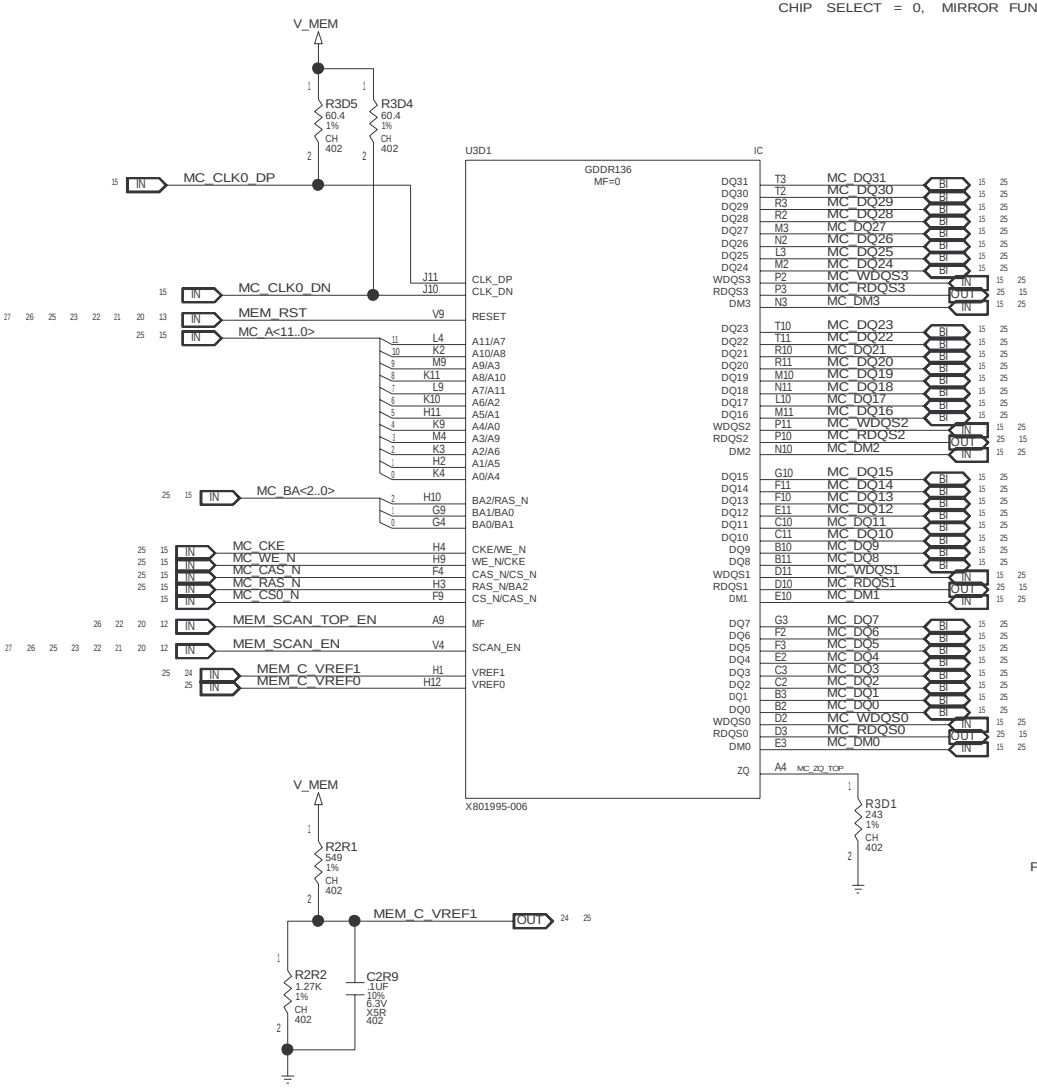
[PAGE_TITLE=MEMORY PARTITION B, BOTTOM]

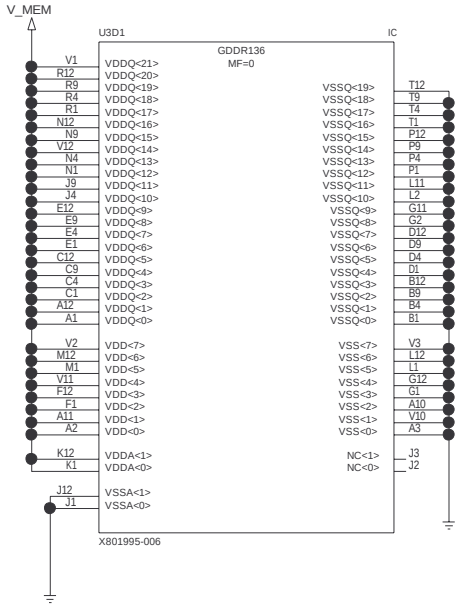
DRAWING
XENON_FABK
Wed Aug 24 09:27:15 2005

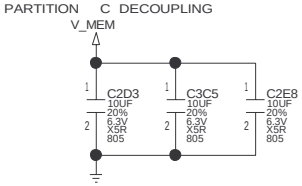
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	23/73	K7

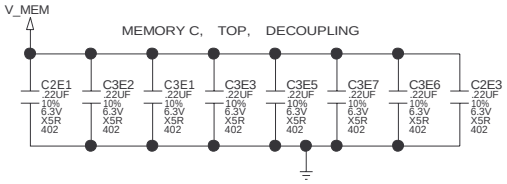
MEMORY PARTITION C, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0









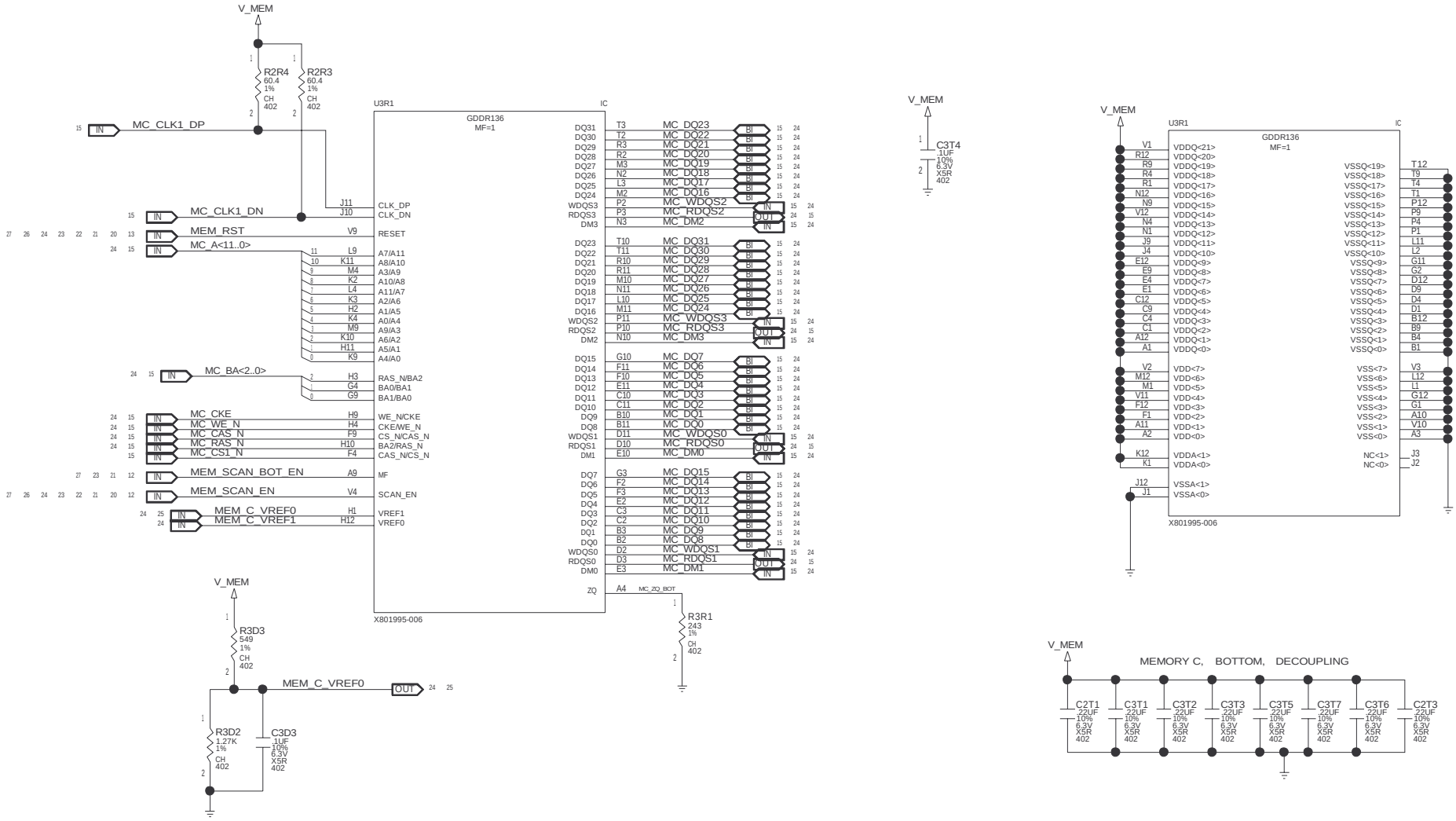
[PAGE_TITLE=MEMORY PARITION C, TOP]

DRAWING
XENON_FABK
Wed Aug 24 09:27:15 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	24/73	K7

MEMORY PARTITION C, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1



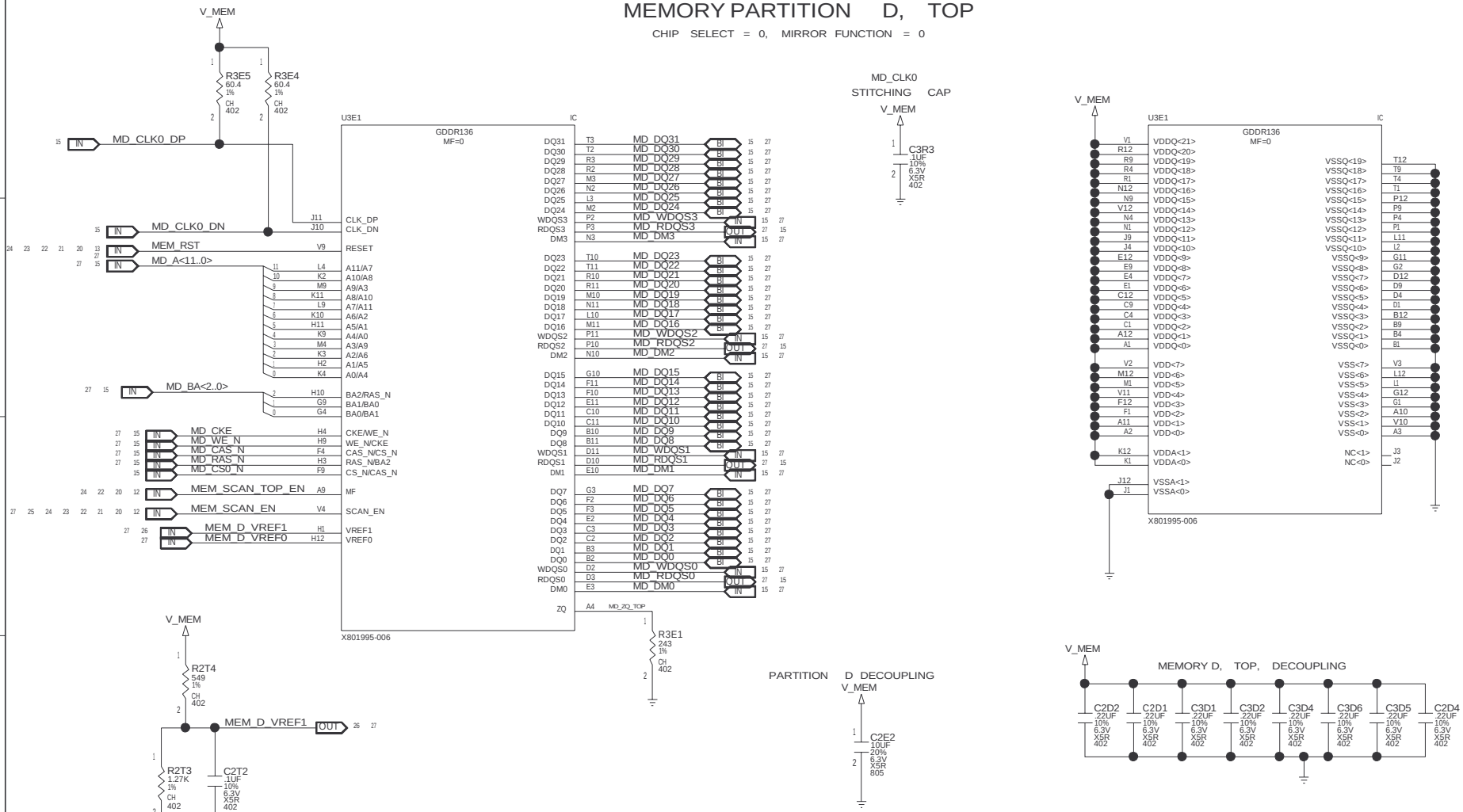
[PAGE_TITLE=MEMORY PARTITION C, BOTTOM]

DRAWING
XENON_FABK
Wed Aug 24 09:27:16 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	25/73	K7

MEMORY PARTITION D, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0



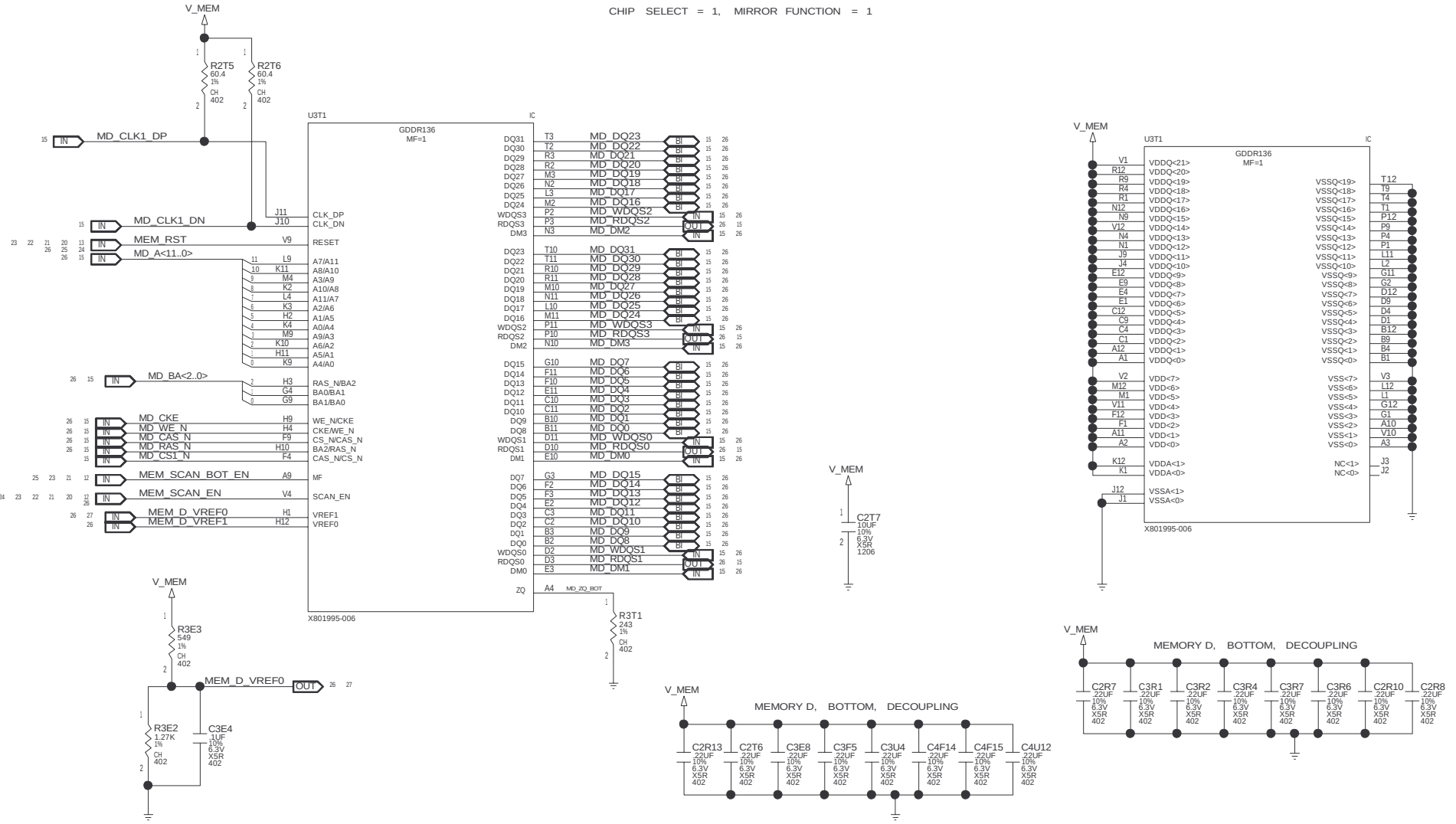
[PAGE_TITLE=MEMORY PARTITION D, TOP]

DRAWING
XENON_FABK
Wed Aug 24 09:27:16 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	26/73	K7

MEMORY PARTITION D, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1

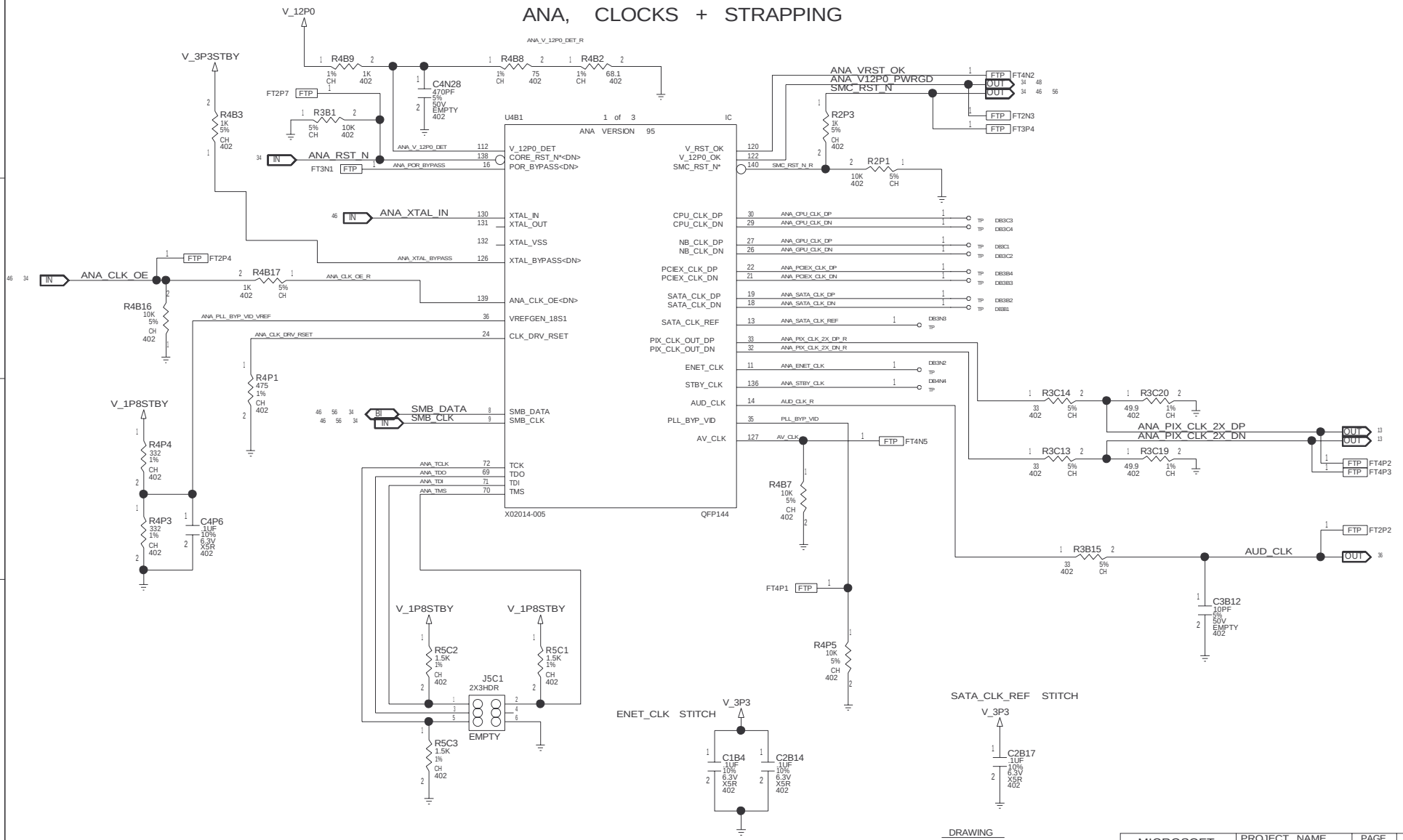


[PAGE_TITLE=MEMORY PARITION D, BOTTOM]

DRAWING
XENON_FABK
Wed Aug 24 09:27:17 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	27/73	K7

ANA, CLOCKS + STRAPPING

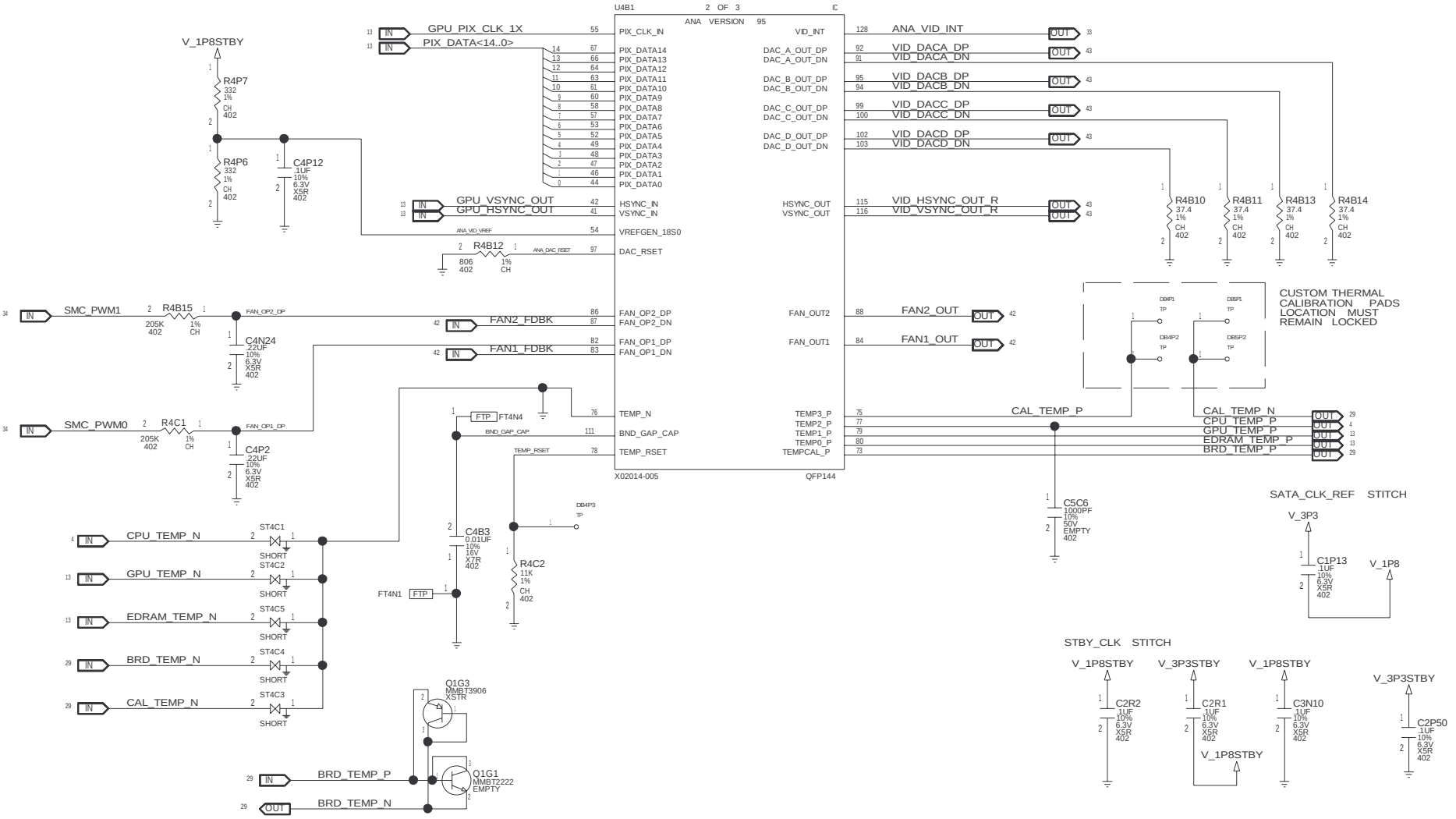


[PAGE_TITLE=ANA, CLOCKS + STRAPPING

DRAWING
XENON_FABK
Wed Aug 24 09:27:18 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	28/73	K7

ANA, VIDEO + FAN + JTAG

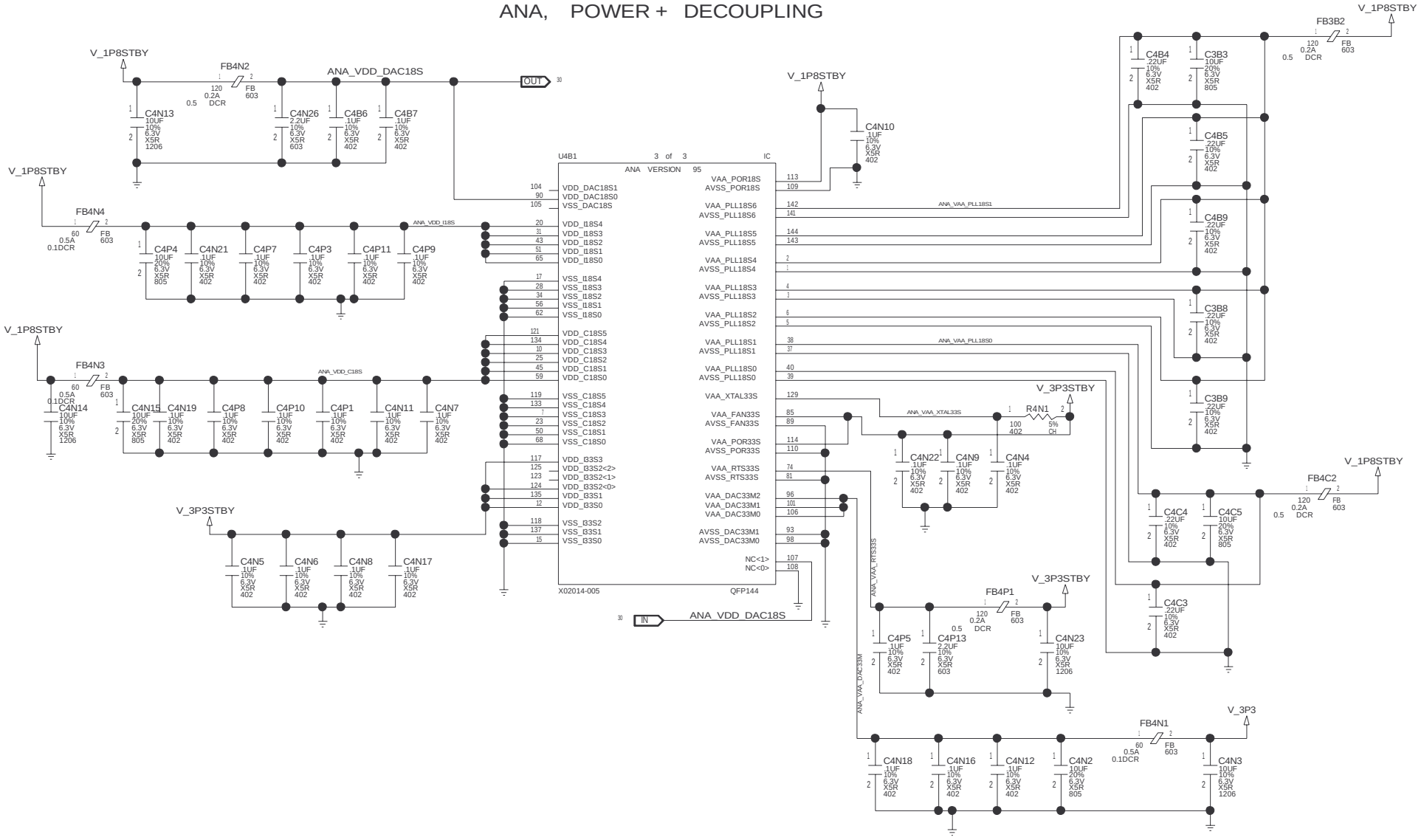


[PAGE_TITLE=ANA, VIDEO + FAN + JTAG]

DRAWING
XENON_FABK
Wed Aug 24 09:27:19 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	29/73	K7

ANA, POWER + DECOUPLING

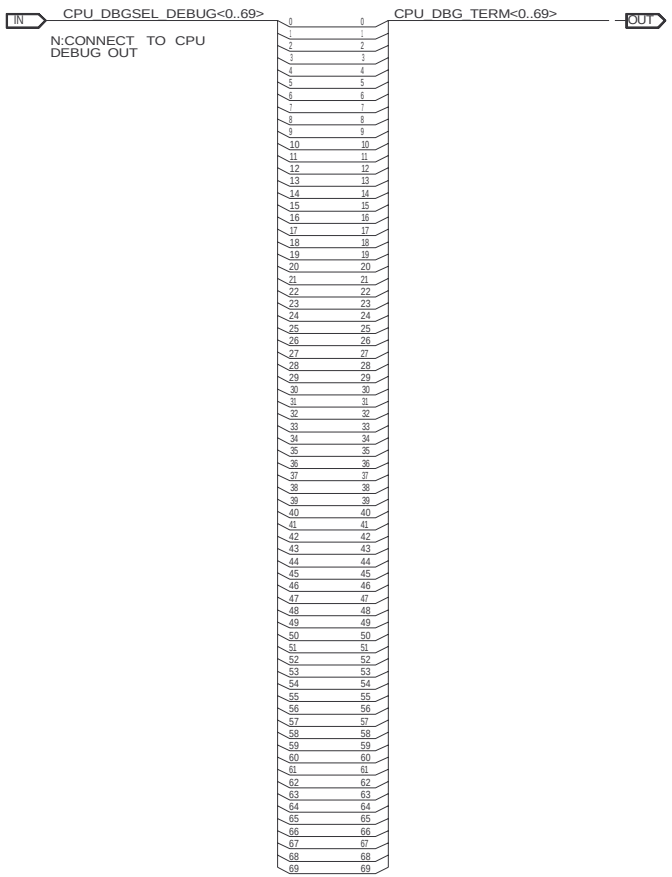


[PAGE_TITLE=ANA, POWER + DECOUPLING]

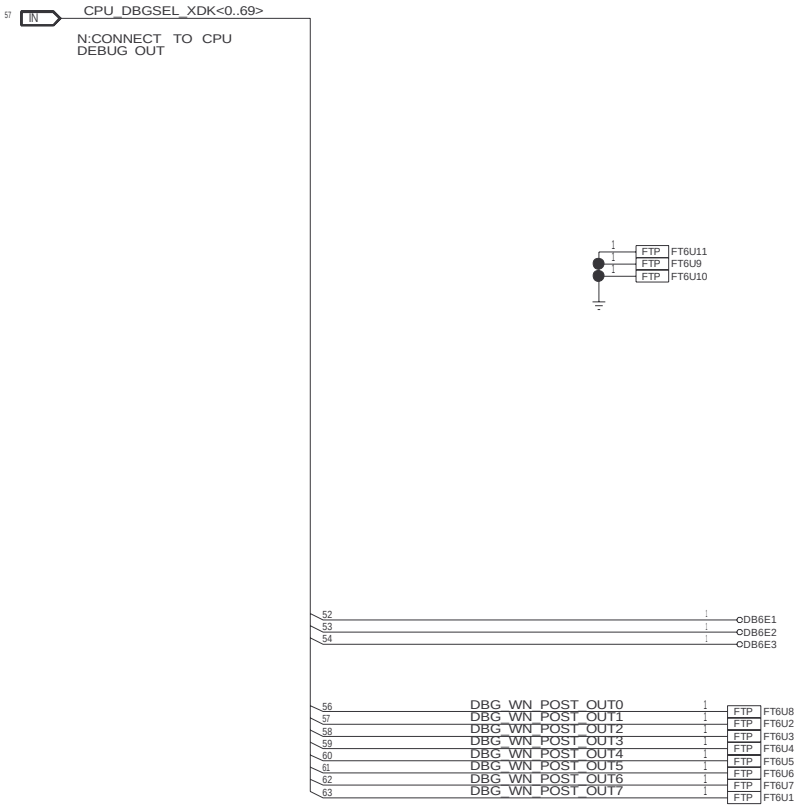
DRAWING
XENON_FABK
Wed Aug 24 09:27:20 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	30/73	K7

DEBUG BOARD MAPPING



XDK BOARD MAPPING

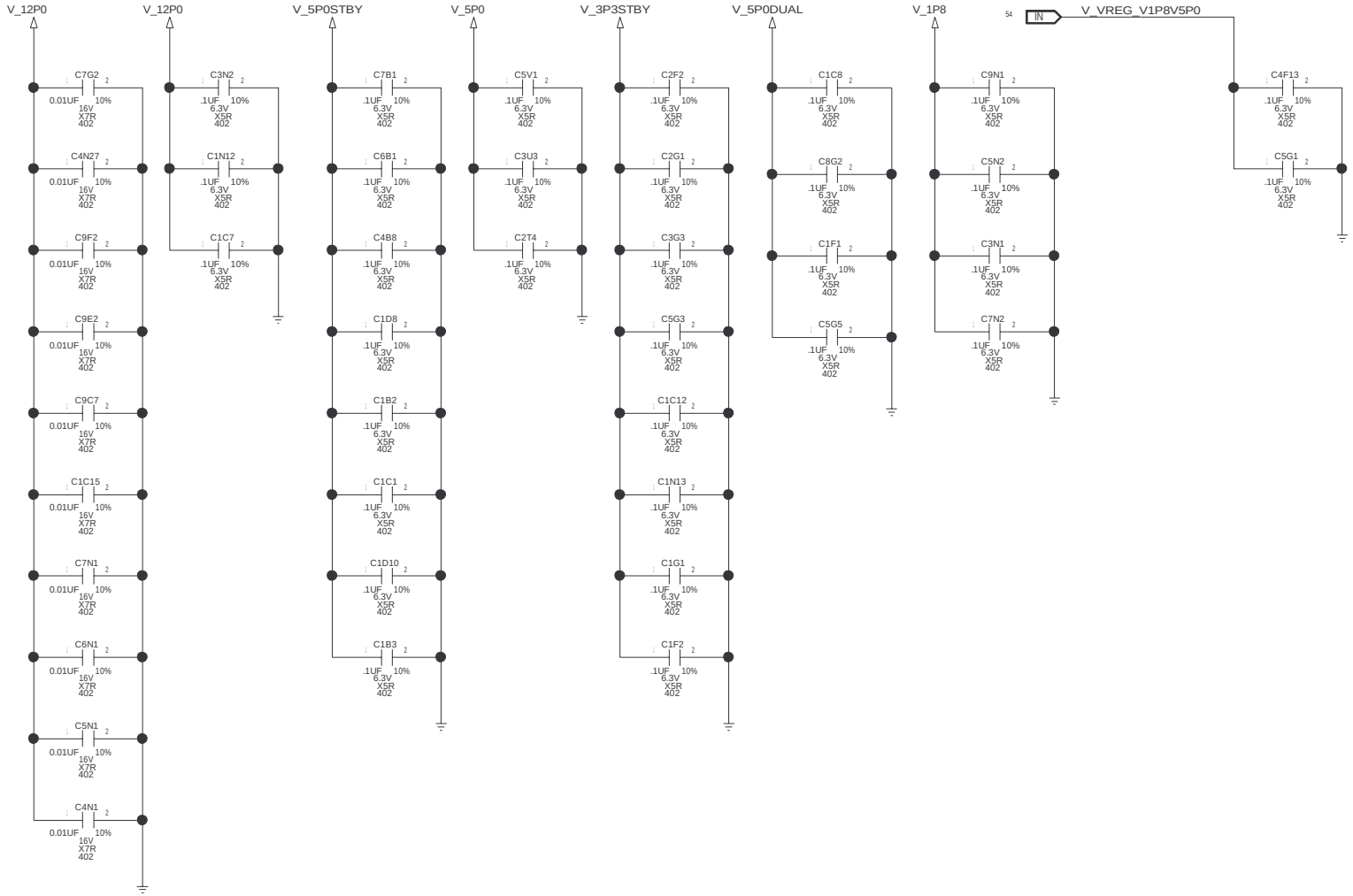


[PAGE_TITLE=DEBUG MAPPING, WN DEBUG VS WN XDK]

DRAWING
XENON_FABK
Wed Aug 24 09:27:21 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	31/73	K7

POWER TRACE DECOUPLING



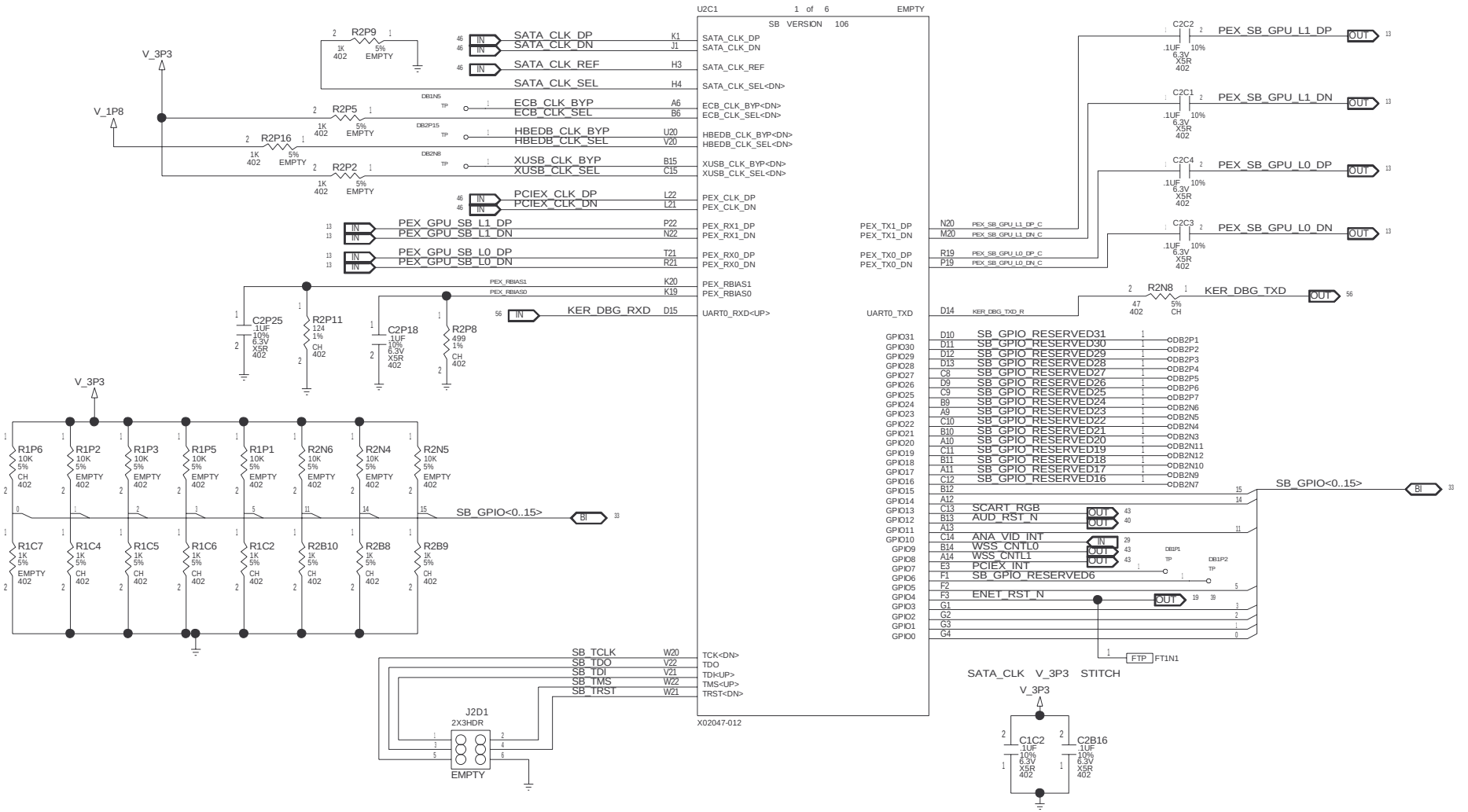
[PAGE_TITLE=POWER TRACE EMI CAPS]

DRAWING
XENON_FABK
Wed Aug 24 09:27:22 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	32/73	K7

ADB:ADD CONFIG TABLE

SB, PCIEX + SMM GPIO + JTAG]

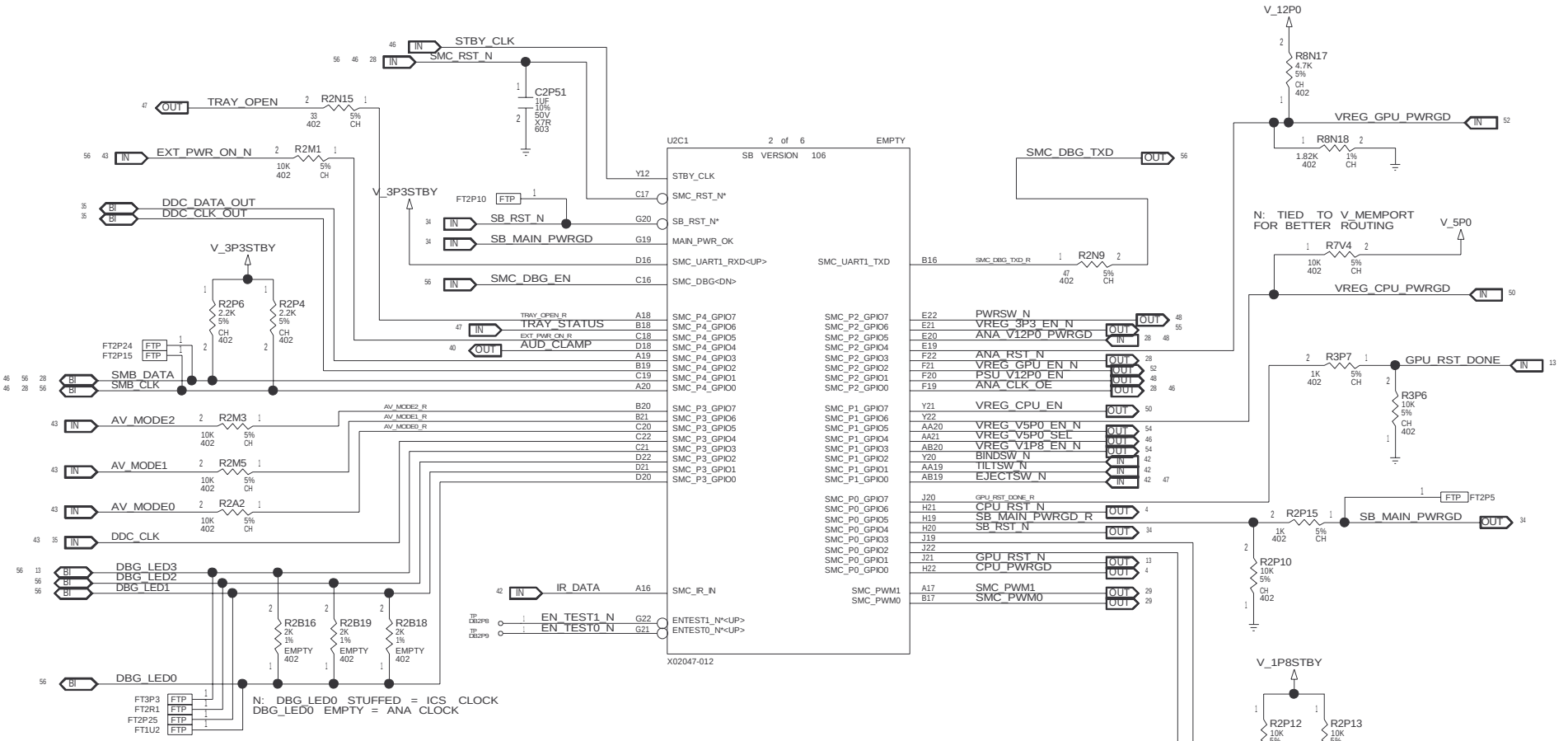


[PAGE_TITLE=SB, PCIEX + SMM GPIO + JTAG]

DRAWING
XENON_FABK
Wed Aug 24 09:27:23 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	33/73	K7

SB, SMC

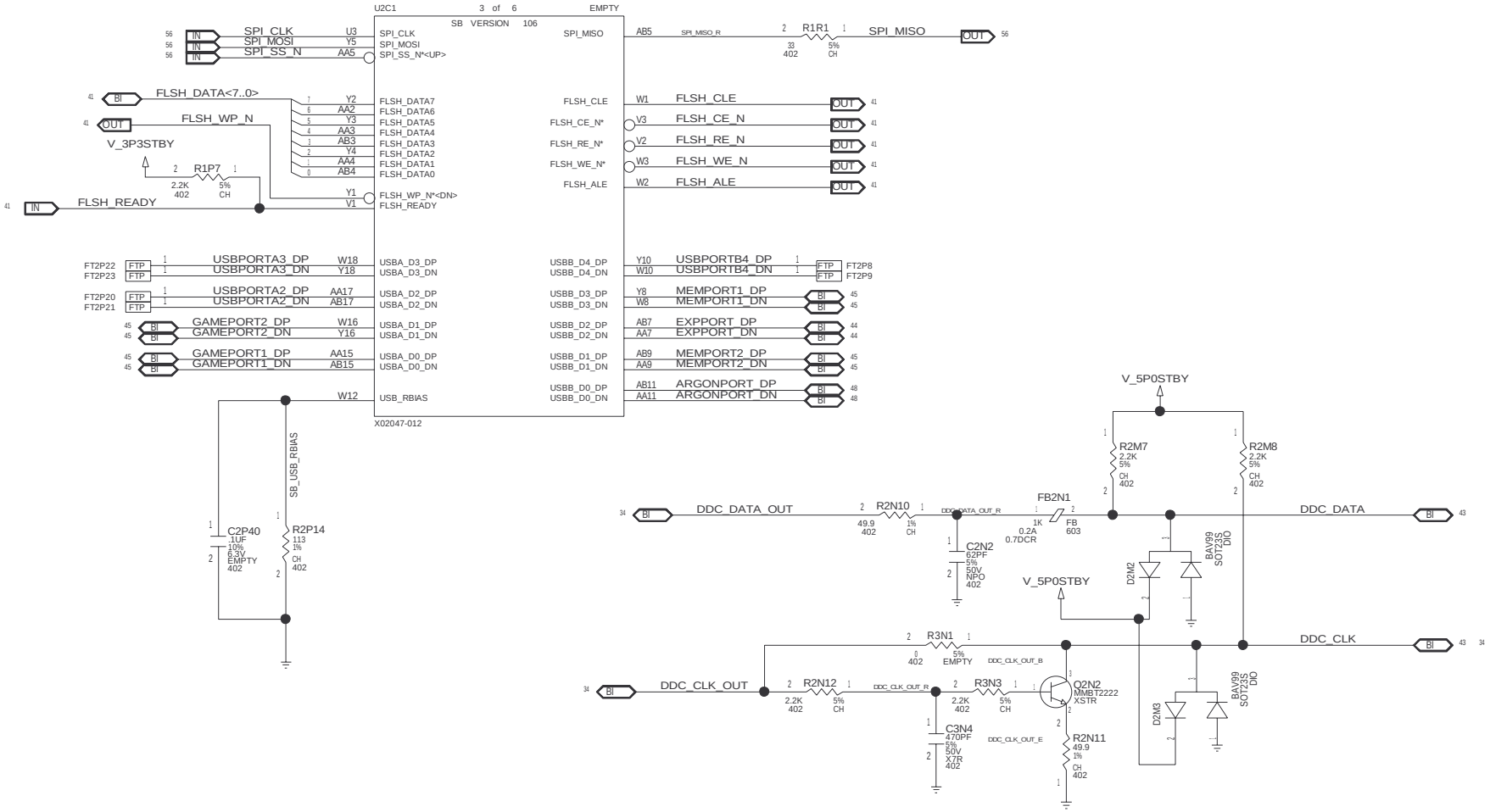


[PAGE_TITLE=SB, SMC]

DRAWING
XENON_FABK
Wed Aug 24 09:27:24 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	34/73	K7

SB, FLASH + USB + SPI

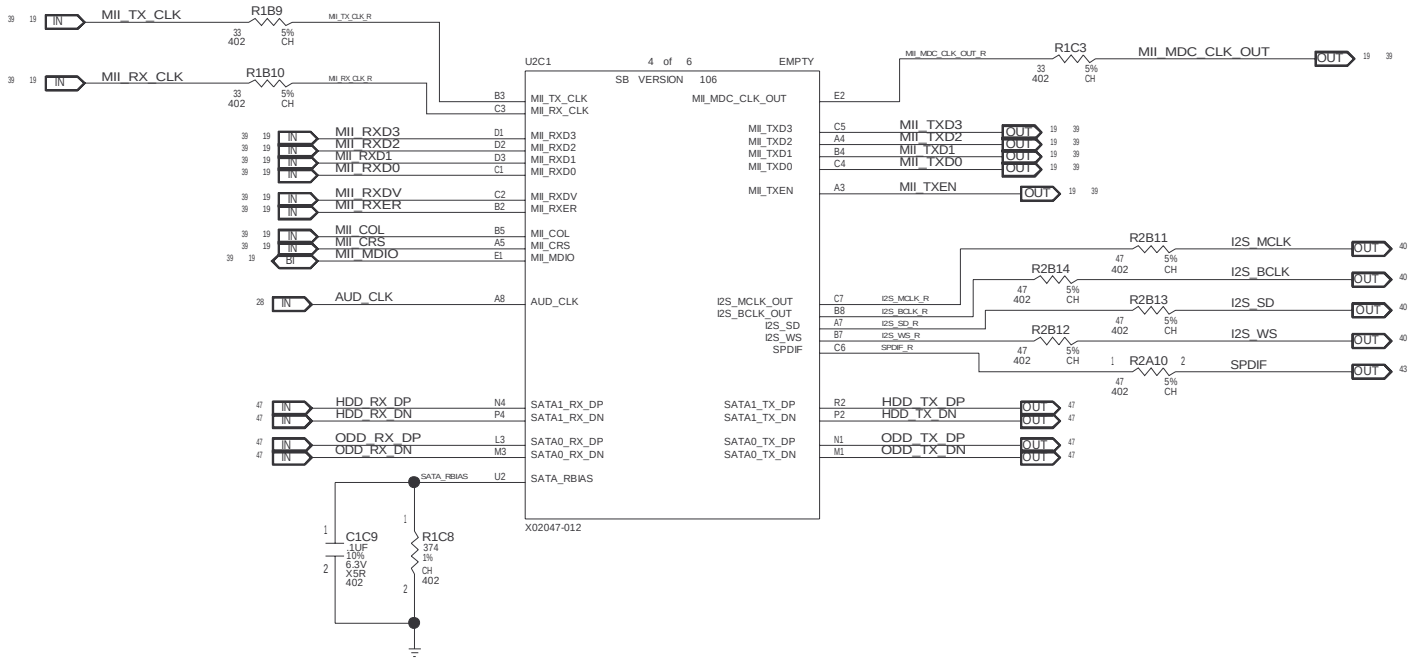


[PAGE_TITLE=SB, FLASH + USB + SPI]

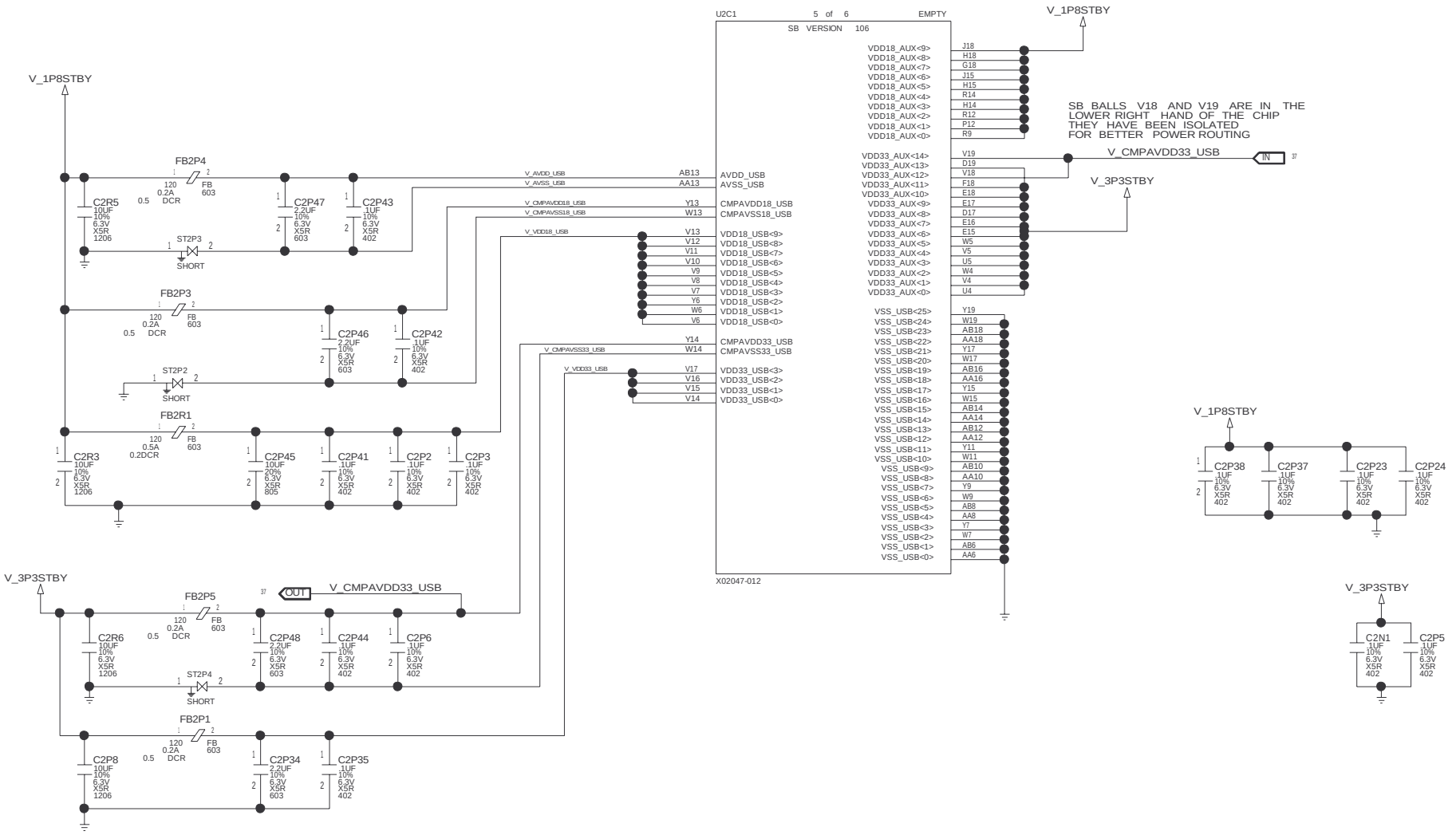
DRAWING
XENON_FABK
Wed Aug 24 09:27:24 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	35/73	K7

SB, ETHERNET + AUDIO + SATA



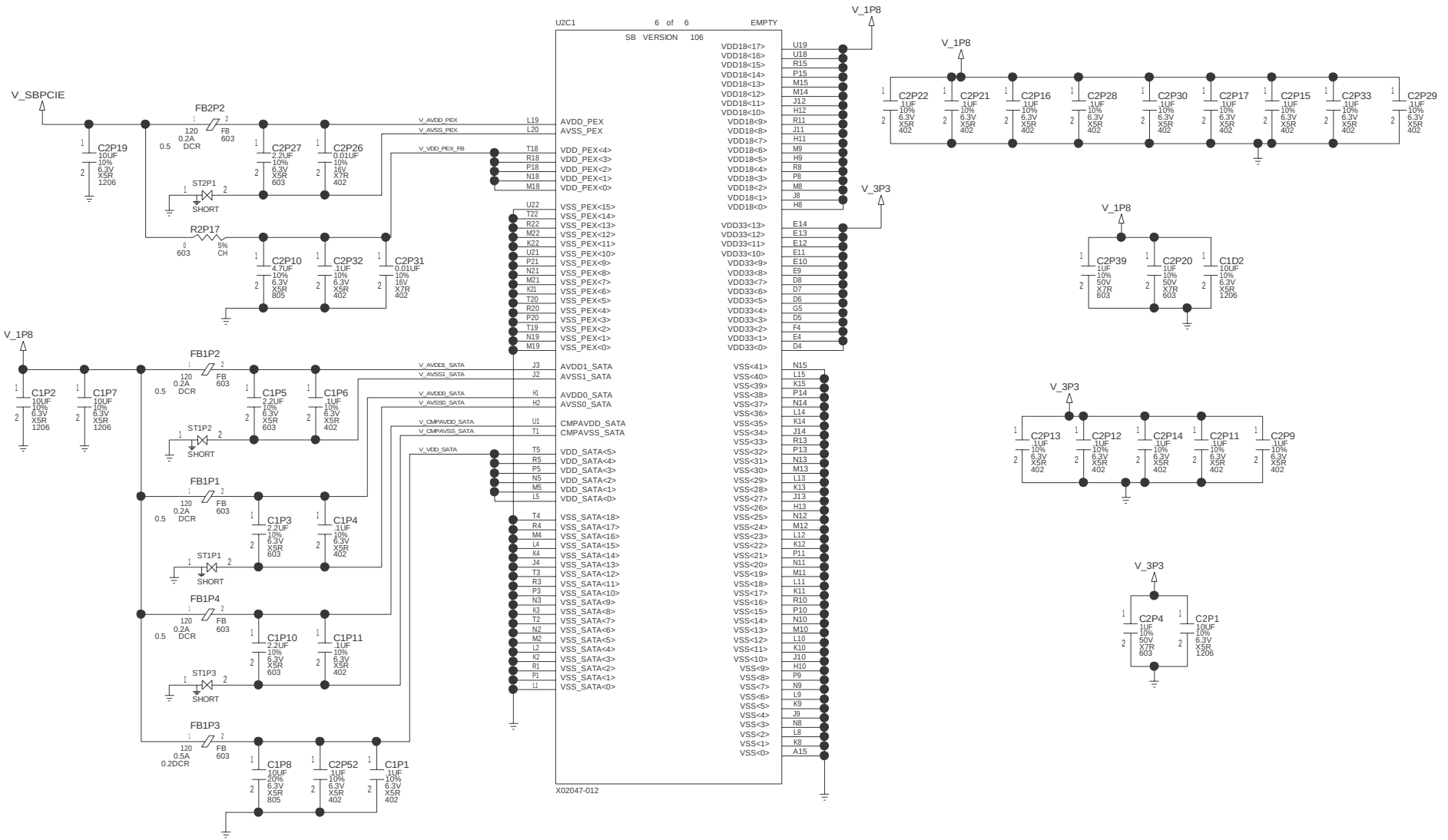
SB, STANDBY POWER + DECOUPLING



[PAGE_TITLE=SB, STANDBY POWER + DECOUPLING]

DRAWING
XENON_FABK
Wed Aug 24 09:27:26 2005

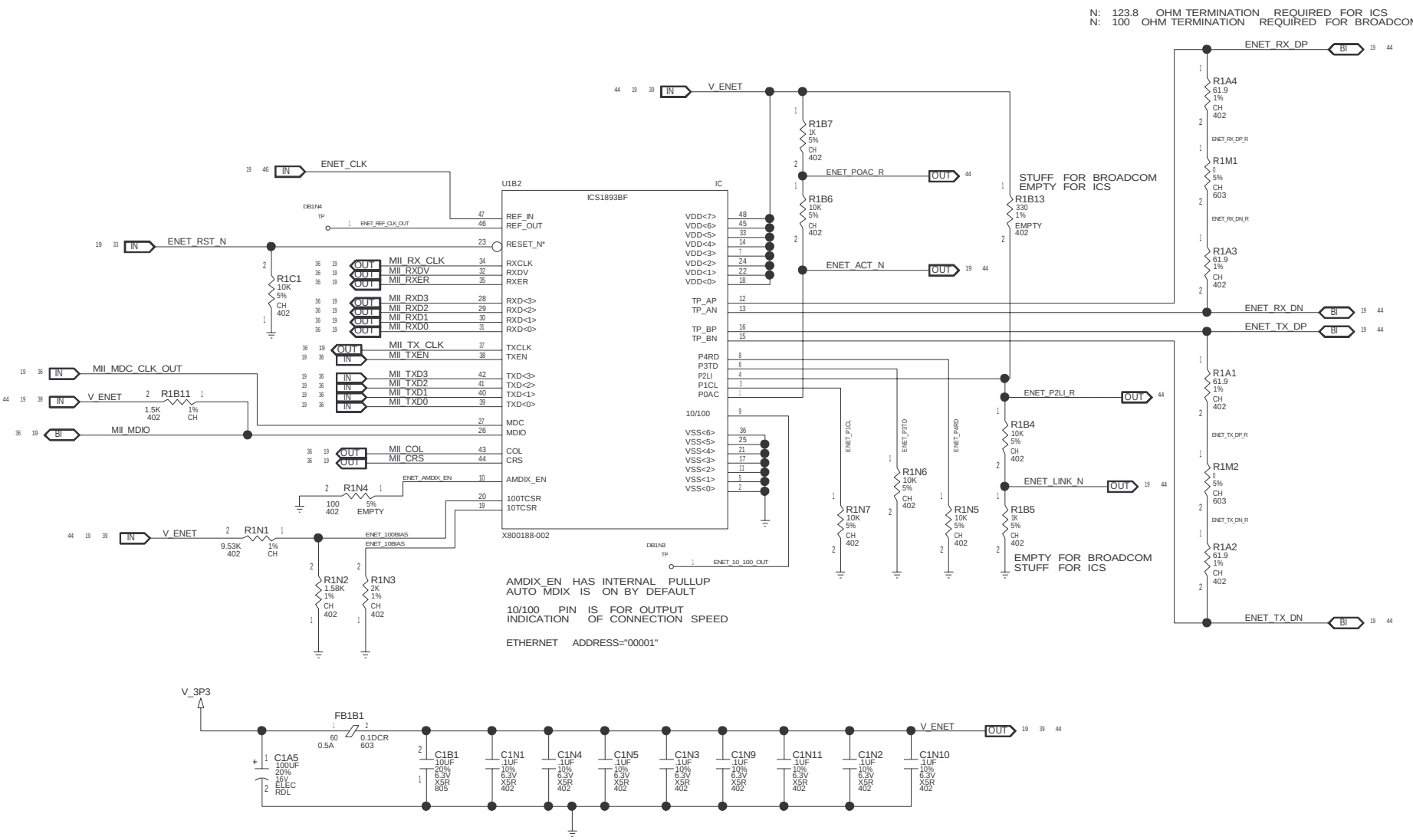
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	37/73	K7



[PAGE_TITLE=SB, MAIN POWER + DECOUPLING]

DRAWING
XENON_FABK
Wed Aug 24 09:27:27 2005

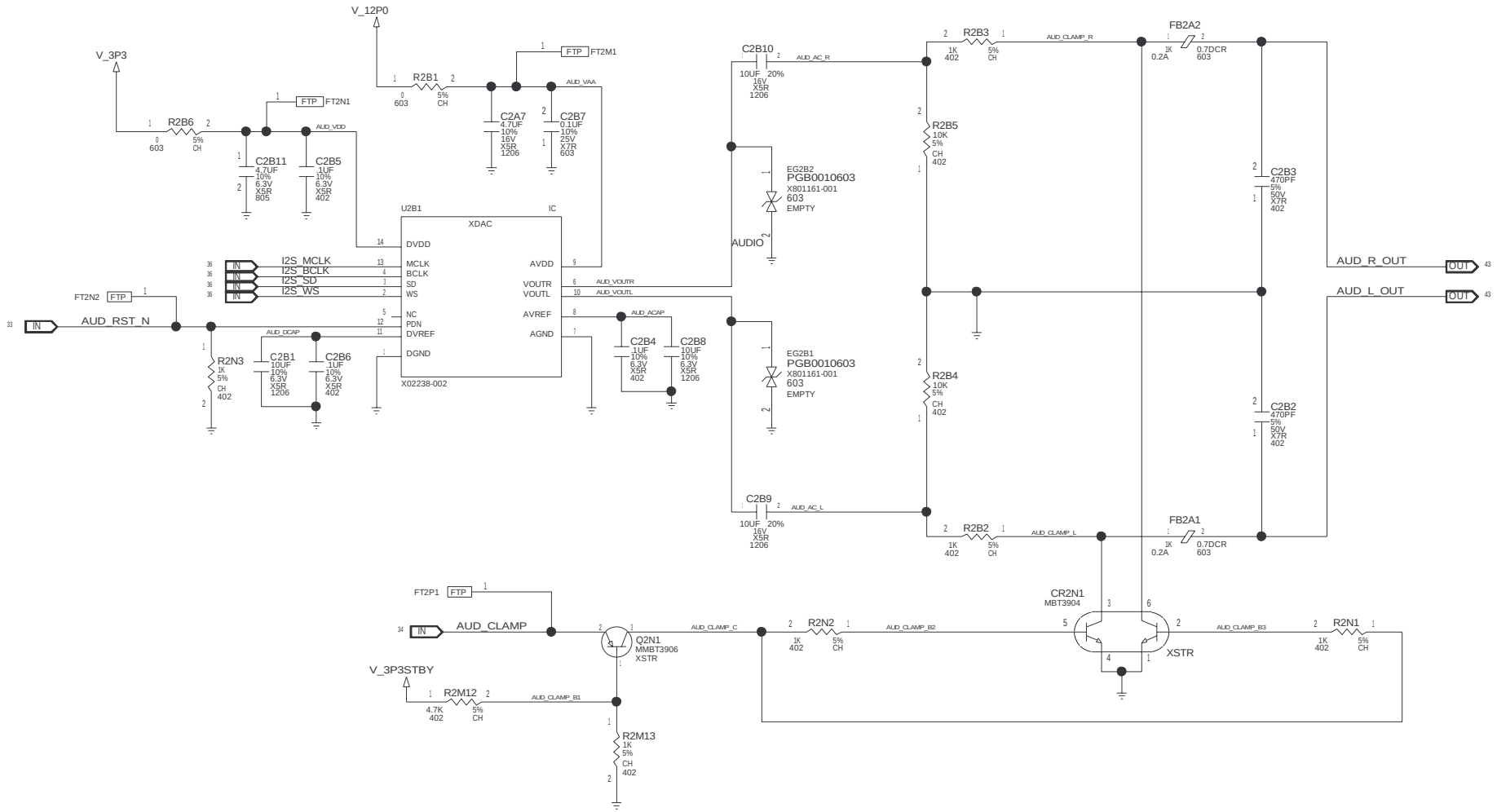
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	38/73	K7



[PAGE_TITLE=SB OUT, ETHERNET]

DRAWING
XENON_FABK
Wed Aug 24 09:27:28 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	39/73	K7



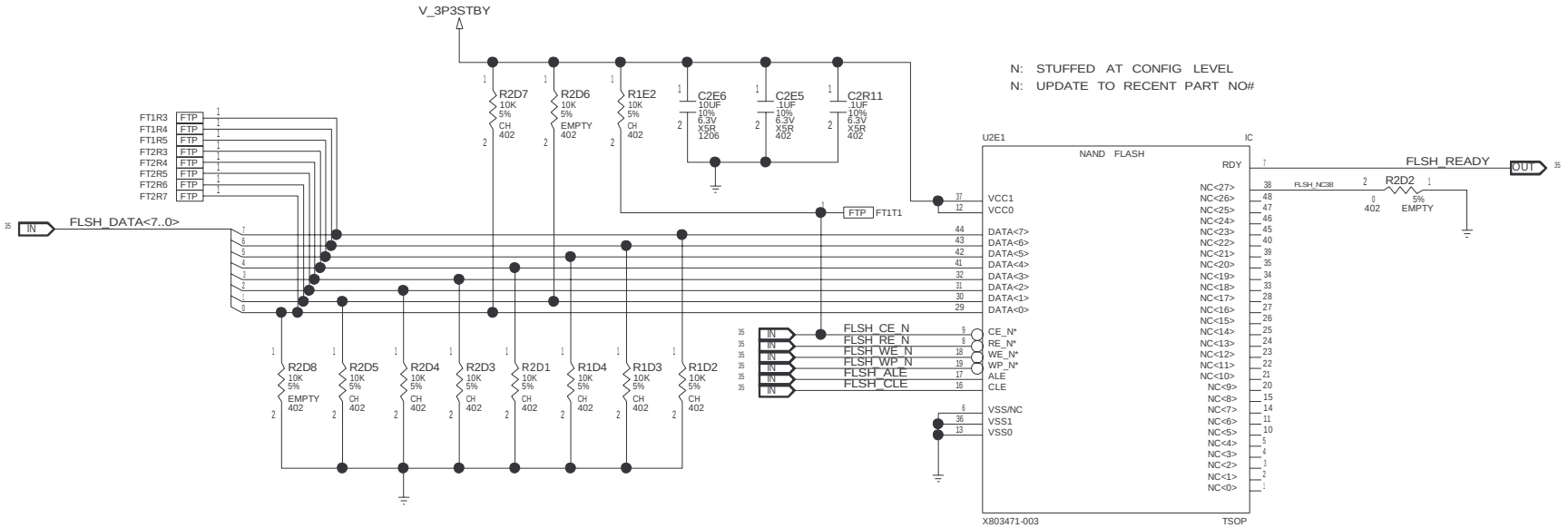
[PAGE_TITLE=SB OUT, AUDIO]

DRAWING
XENON_FABK
Wed Aug 24 09:27:29 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	40/73	K7

FLSH_DATA1 \ FLSH_DATA0	0	1
0	8MB	16MB
1	32MB	64MB

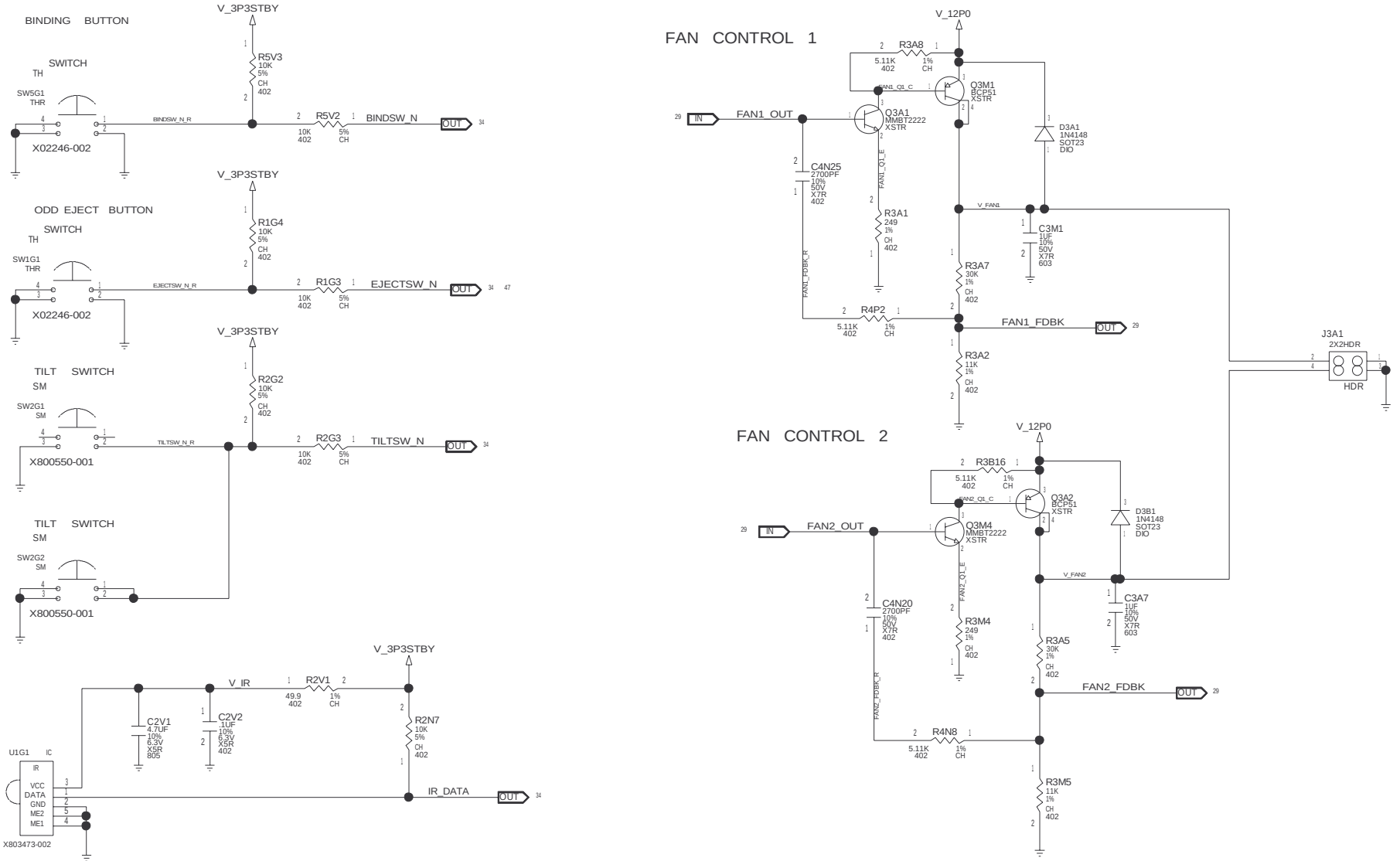
N: RETAIL=16MB
N: XDK=64MB



[PAGE_TITLE=SB OUT, FLASH]

DRAWING
XENON_FABK
Wed Aug 24 09:27:30 2005

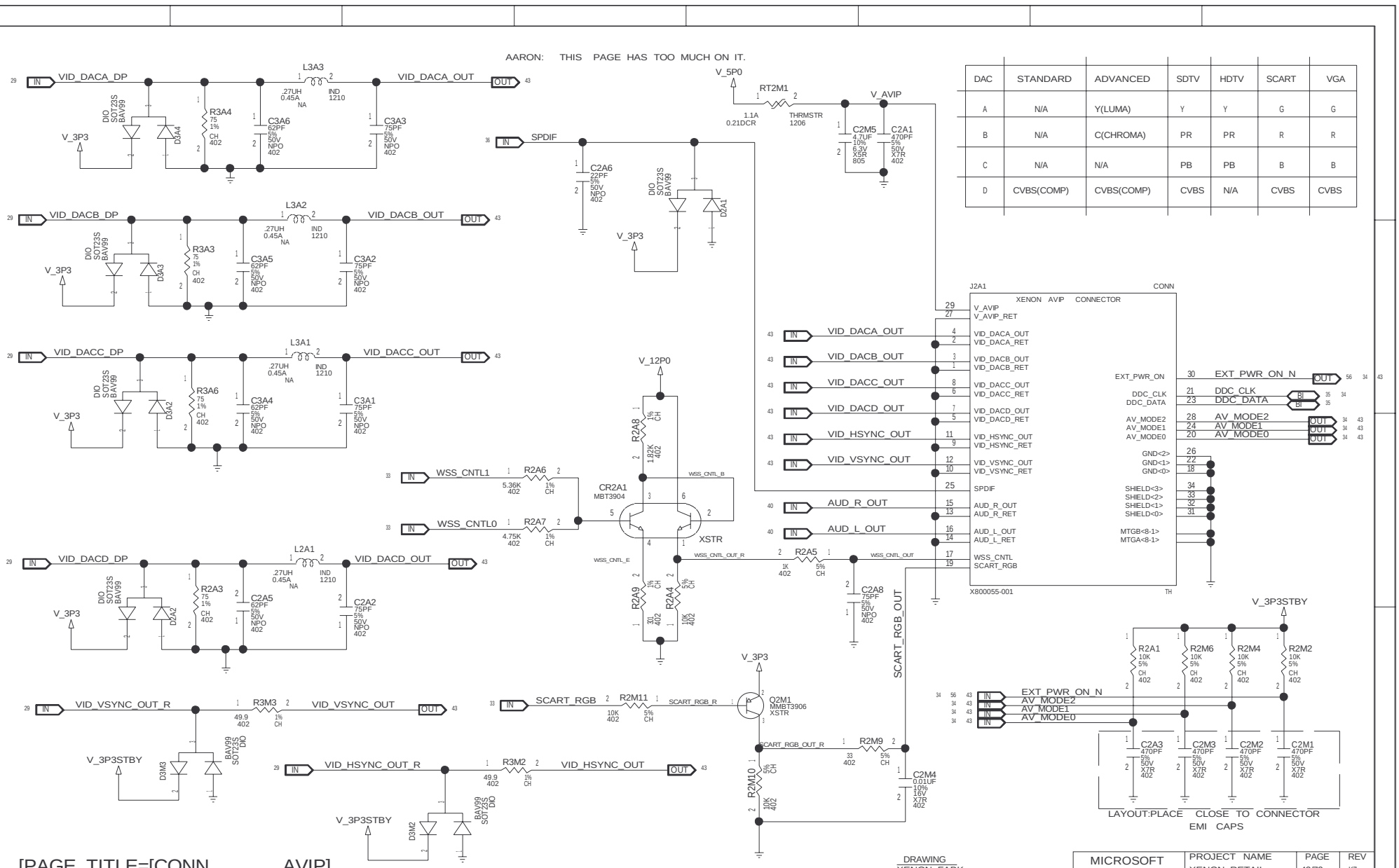
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	41/73	K7



[PAGE_TITLE=CONN, FAN + INFRARED + SWITCHES]

DRAWING
XENON_FABK
Wed Aug 24 09:27:30 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	42/73	K7



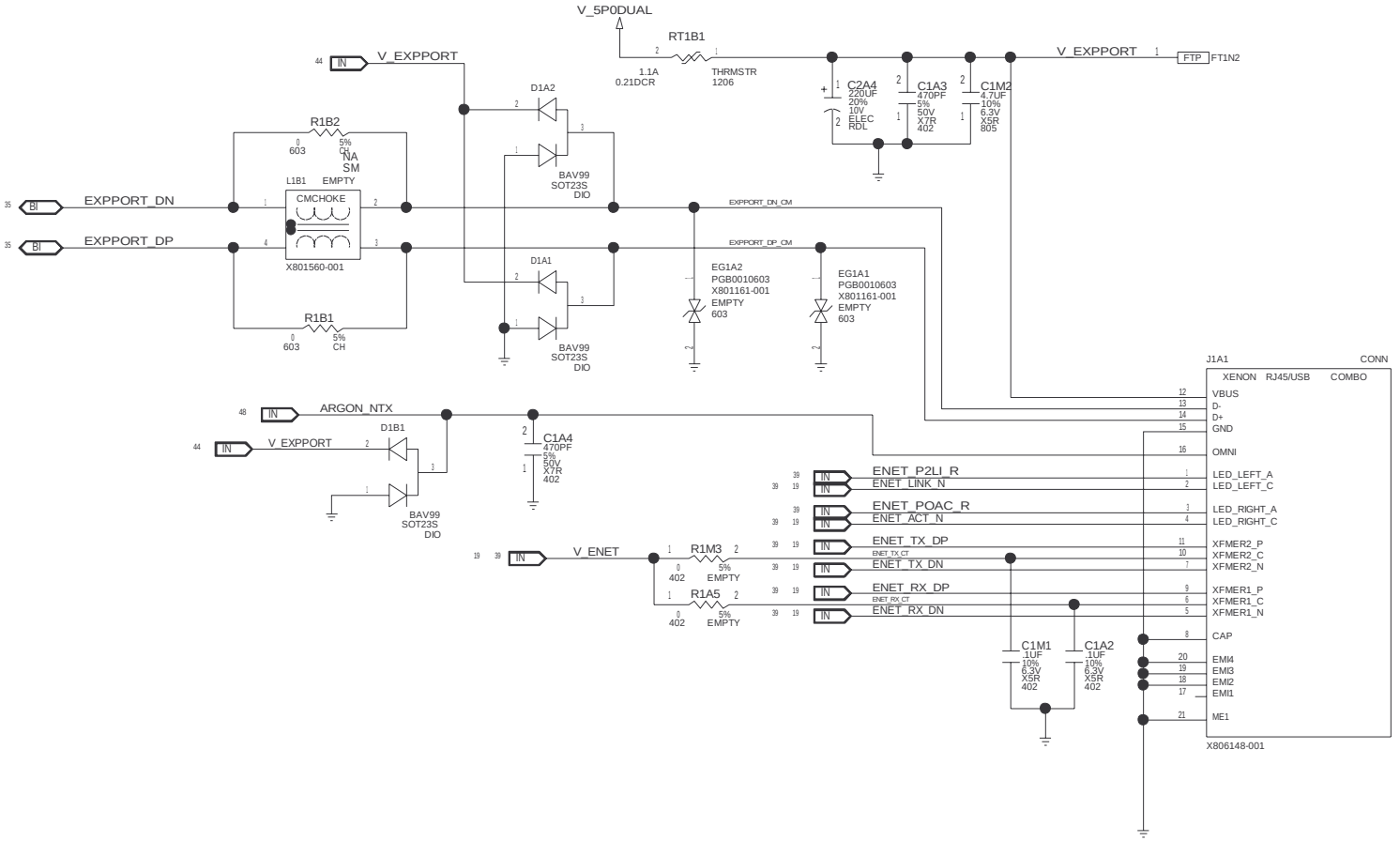
DAC	STANDARD	ADVANCED	SDTV	HDTV	SCART	VGA
A	N/A	Y(LUMA)	Y	Y	G	G
B	N/A	C(CHROMA)	PR	PR	R	R
C	N/A	N/A	PB	PB	B	B
D	CVBS(COMP)	CVBS(COMP)	CVBS	N/A	CVBS	CVBS

[PAGE_TITLE=[CONN, AVIP]

DRAWING
XENON_FABK
Wed Aug 24 09:27:31 2005

MICROSOFT CONFIDENTIAL

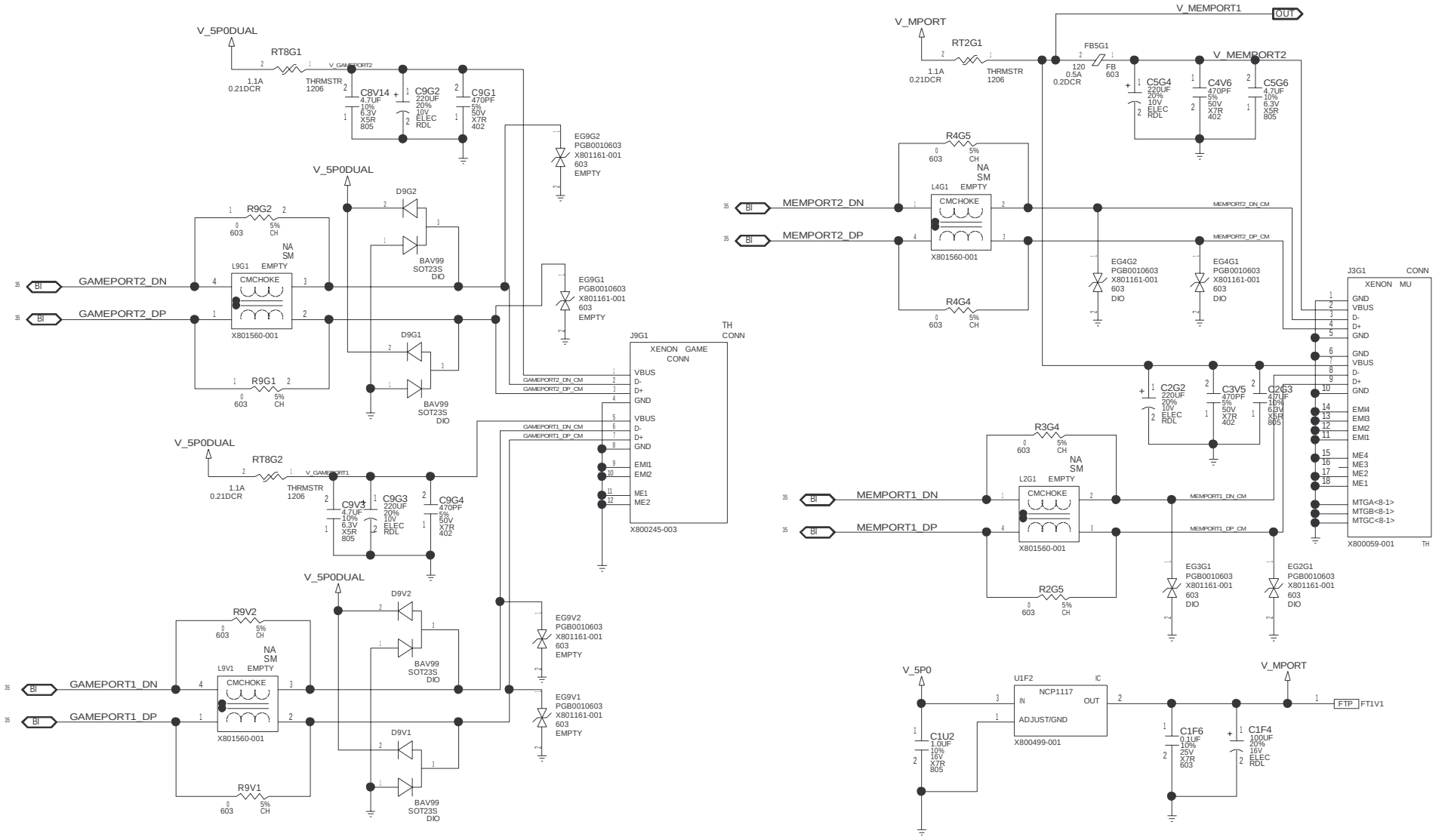
PROJECT NAME	PAGE	REV
XENON_RETAIL	43/73	K7



[PAGE_TITLE=CONN, ETHERNET]

DRAWING
XENON_FABK
Wed Aug 24 09:27:32 2005

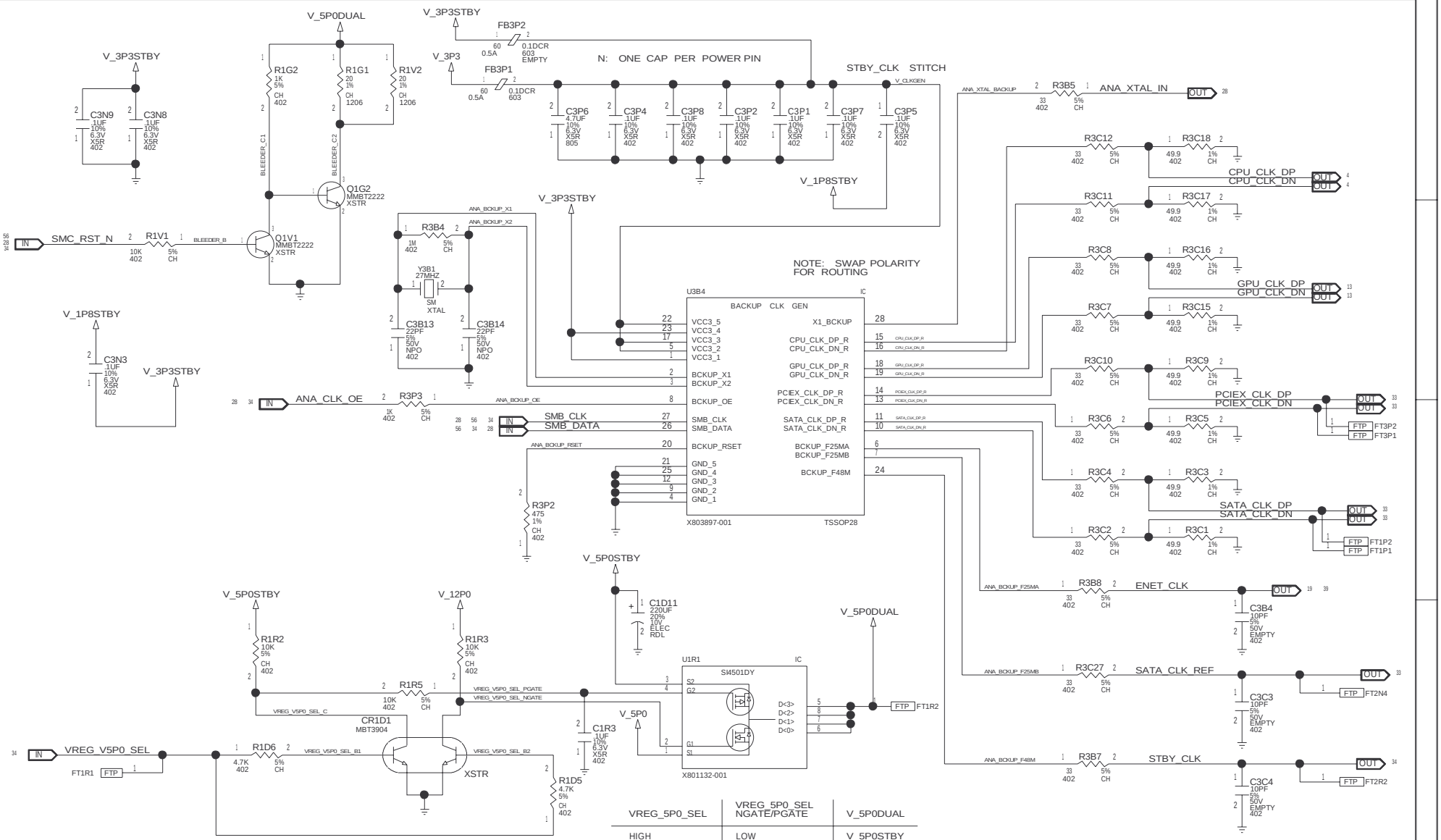
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	44/73	K7



[PAGE_TITLE=CONN, MEMORY PORTS + GAME PORTS]

DRAWING
XENON_FABK
Wed Aug 24 09:27:33 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	45/73	K7

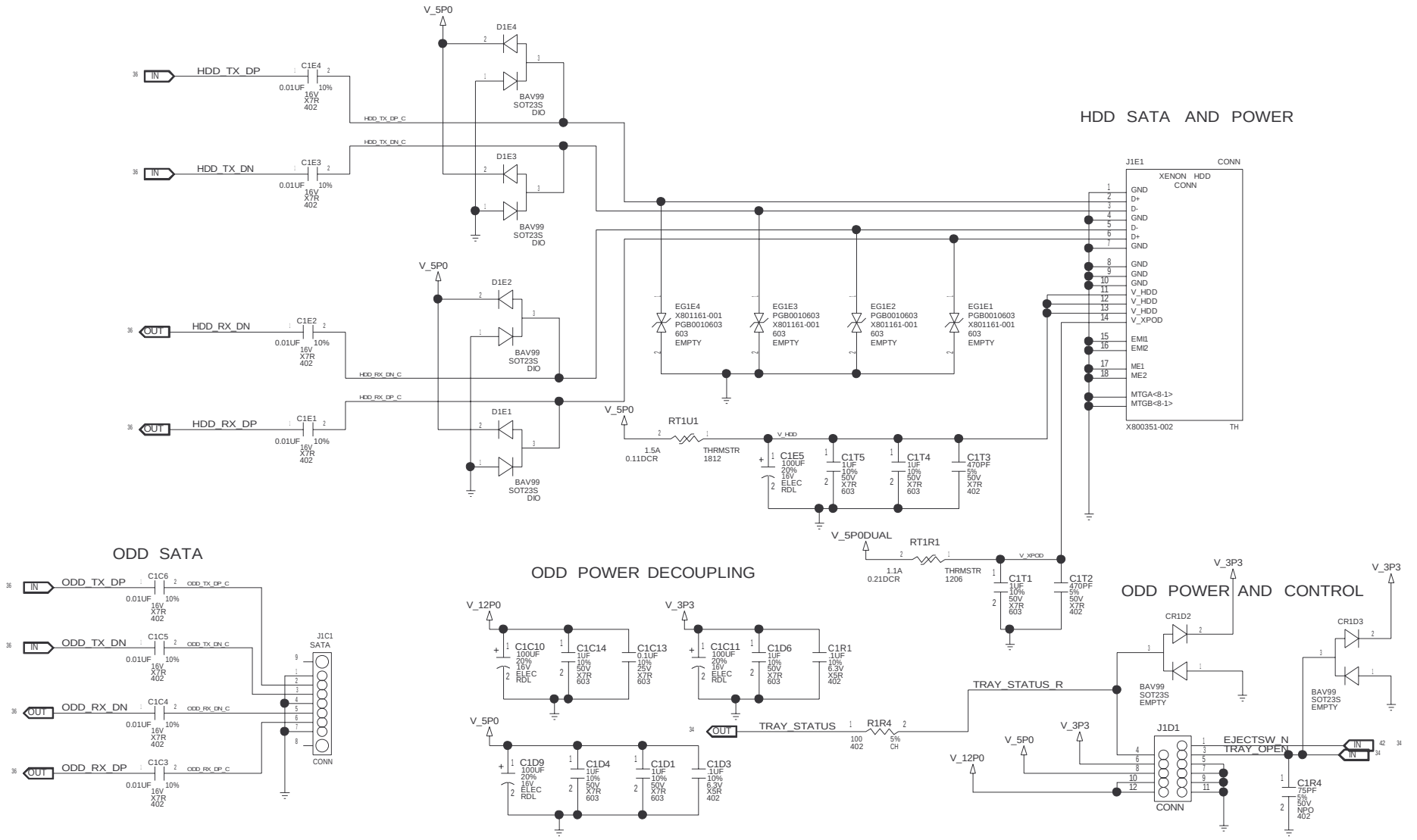


VREG_5P0_SEL	VREG_5P0_SEL NGATE/PGATE	V_5P0DUAL
HIGH	LOW	V_5P0STBY
LOW	HIGH	V_5P0

[PAGE_TITLE=[BACKUP CLOCK + V_5P0 DUAL]

DRAWING
XENON_FABK
Wed Aug 24 09:27:34 2005

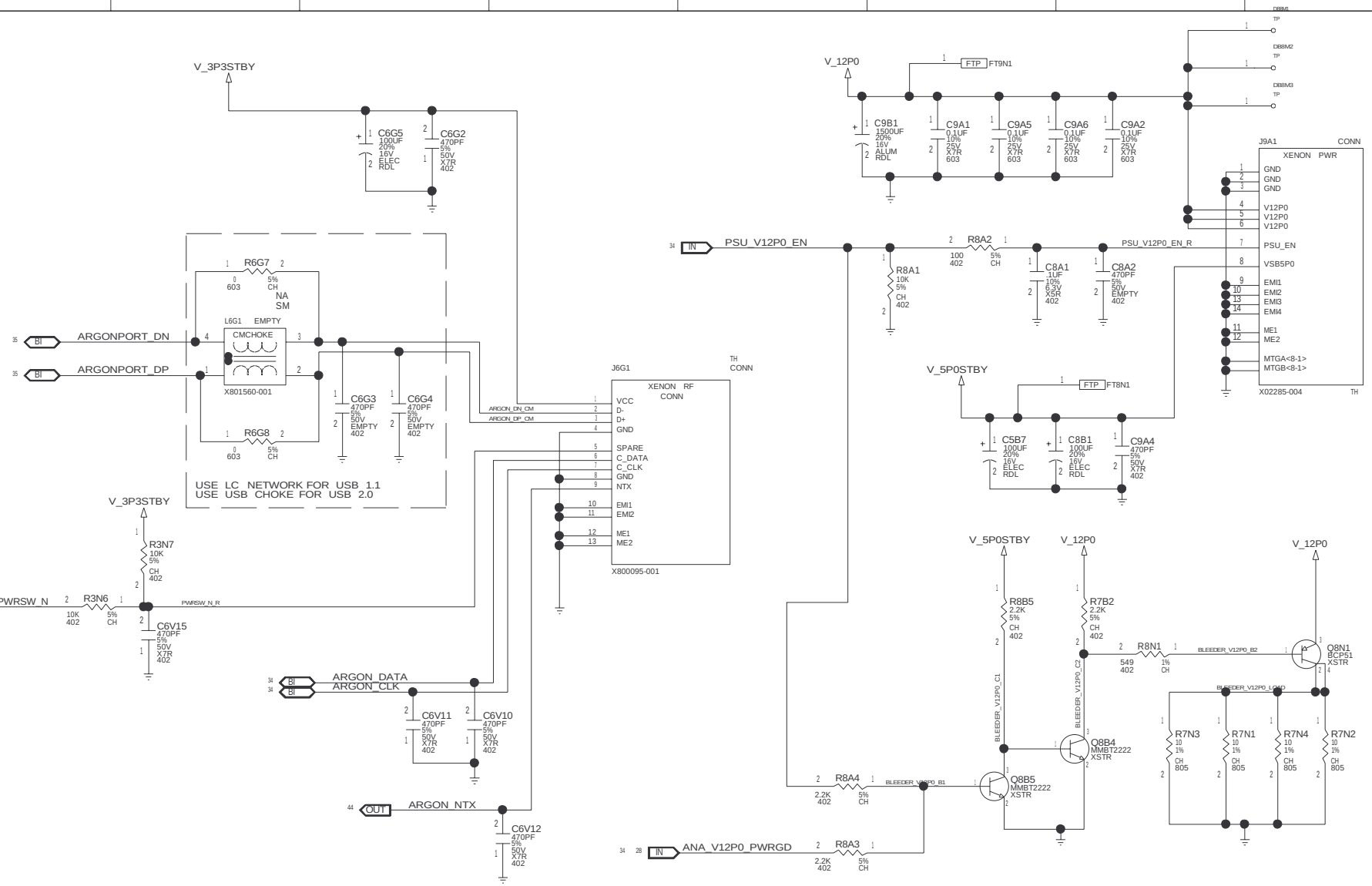
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	46/73	K7



[PAGE_TITLE=CONN, ODD + HDD]

DRAWING
XENON_FABK
Wed Aug 24 09:27:35 2005

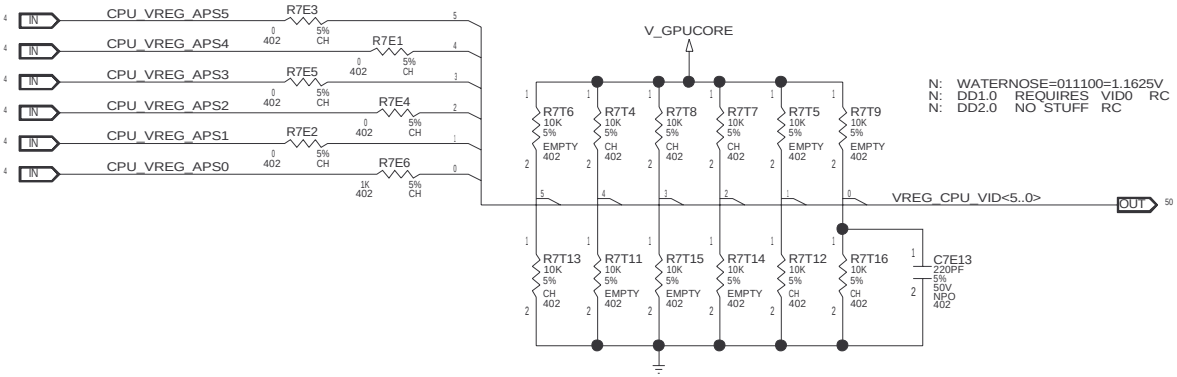
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	47/73	K7

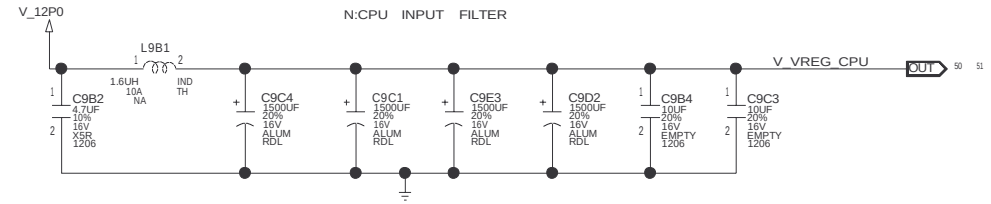


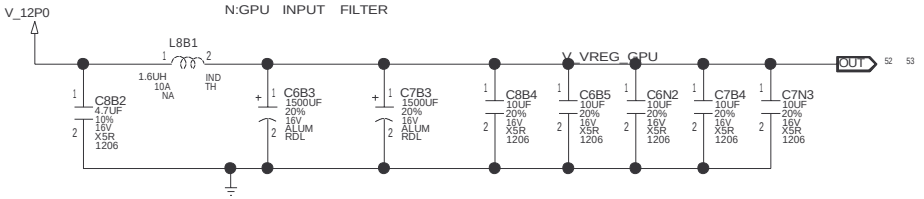
[PAGE_TITLE=CONN, ARGON + POWER]

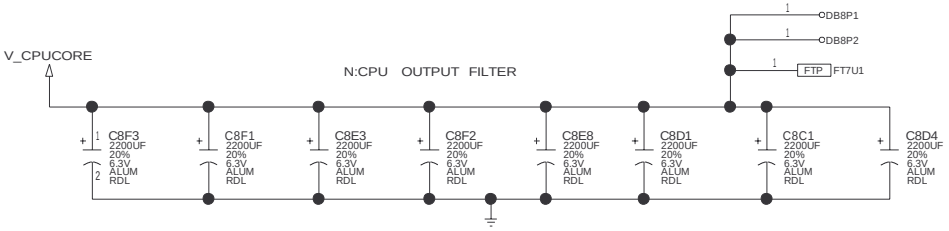
DRAWING
XENON_FABK
Wed Aug 24 09:27:35 2005

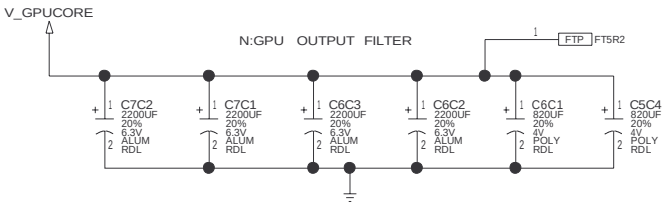
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	48/73	K7







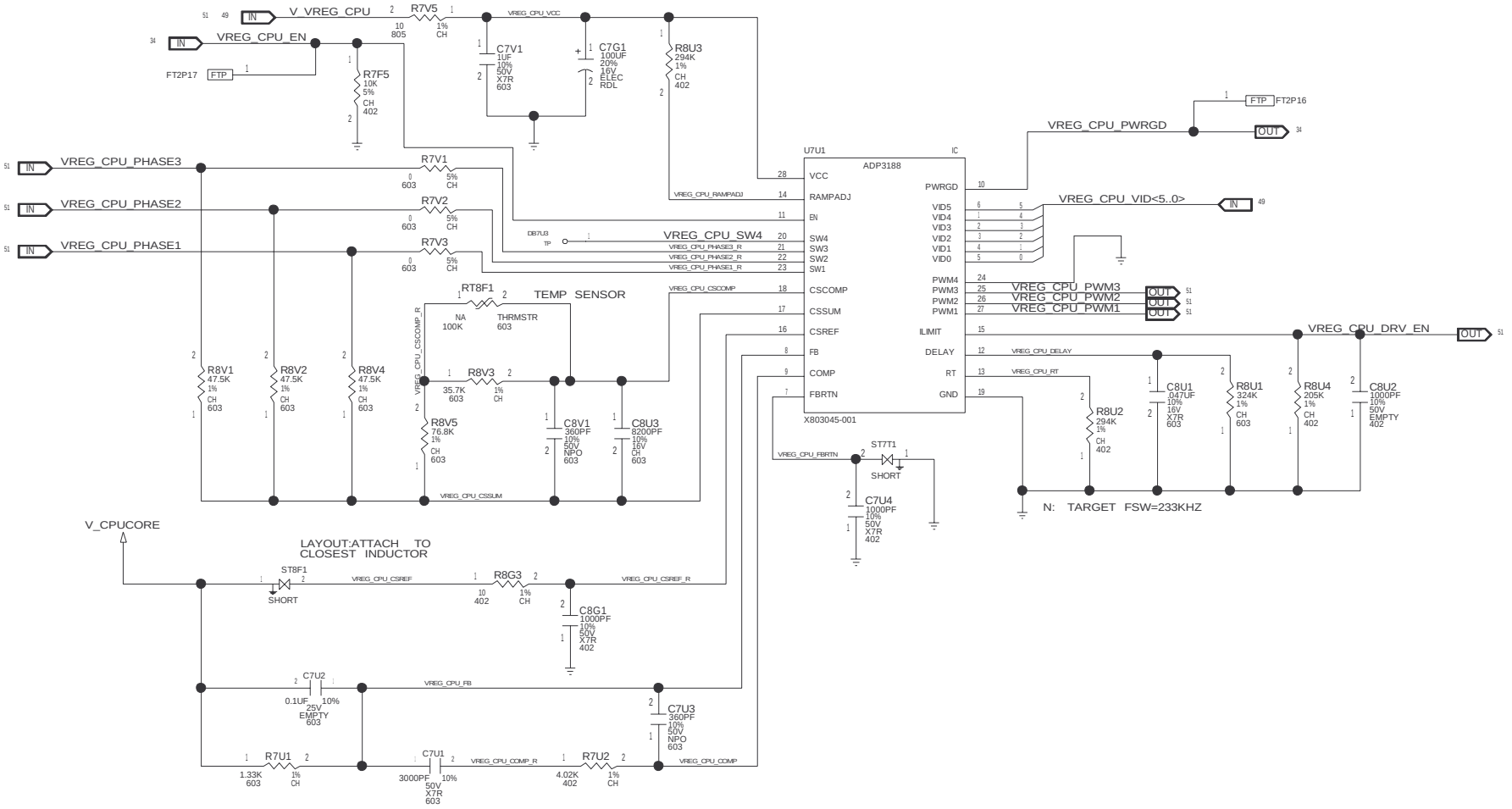




[PAGE_TITLE=VREGS, INPUT + OUTPUT FILTERS]

DRAWING
XENON_FABK
Wed Aug 24 09:27:36 2005

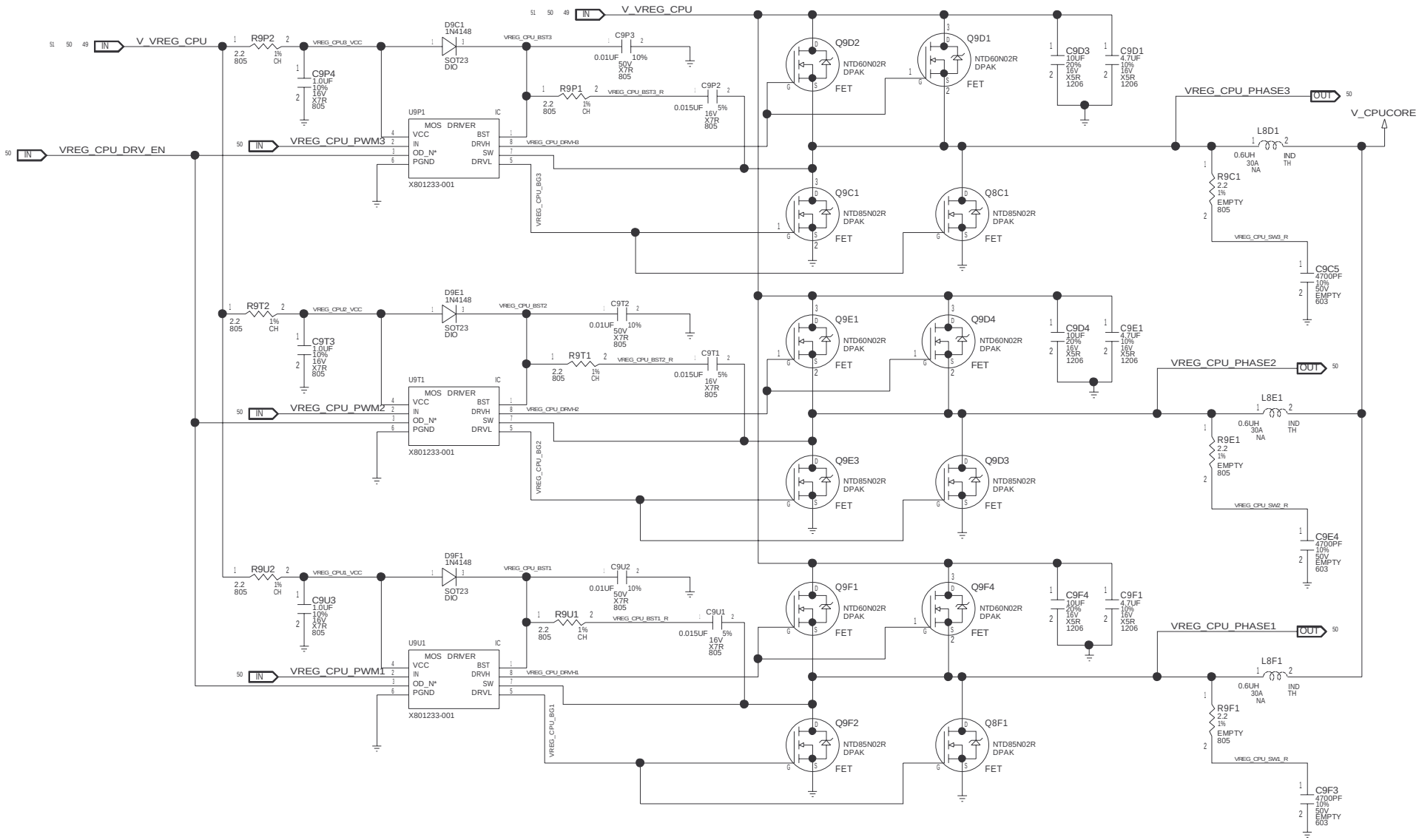
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	49/73	K7



[PAGE_TITLE=VREGS, CPU CONTROLLER]

DRAWING
XENON_FABK
Wed Aug 24 09:27:36 2005

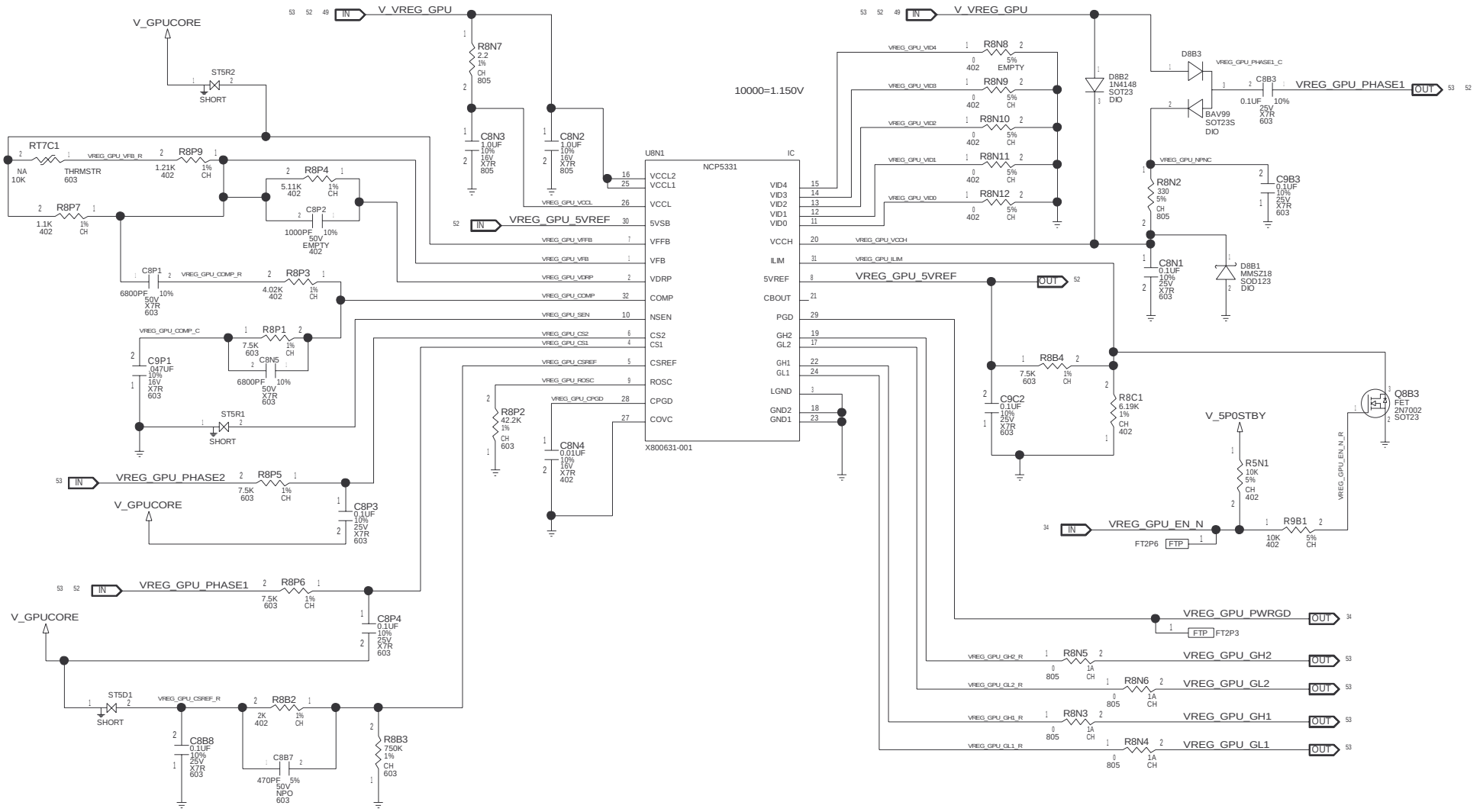
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	50/73	K7



[PAGE_TITLE=VREGS, CPU OUTPUT PHASE 1,2,3]

DRAWING
XENON_FABK
Wed Aug 24 09:27:37 2005

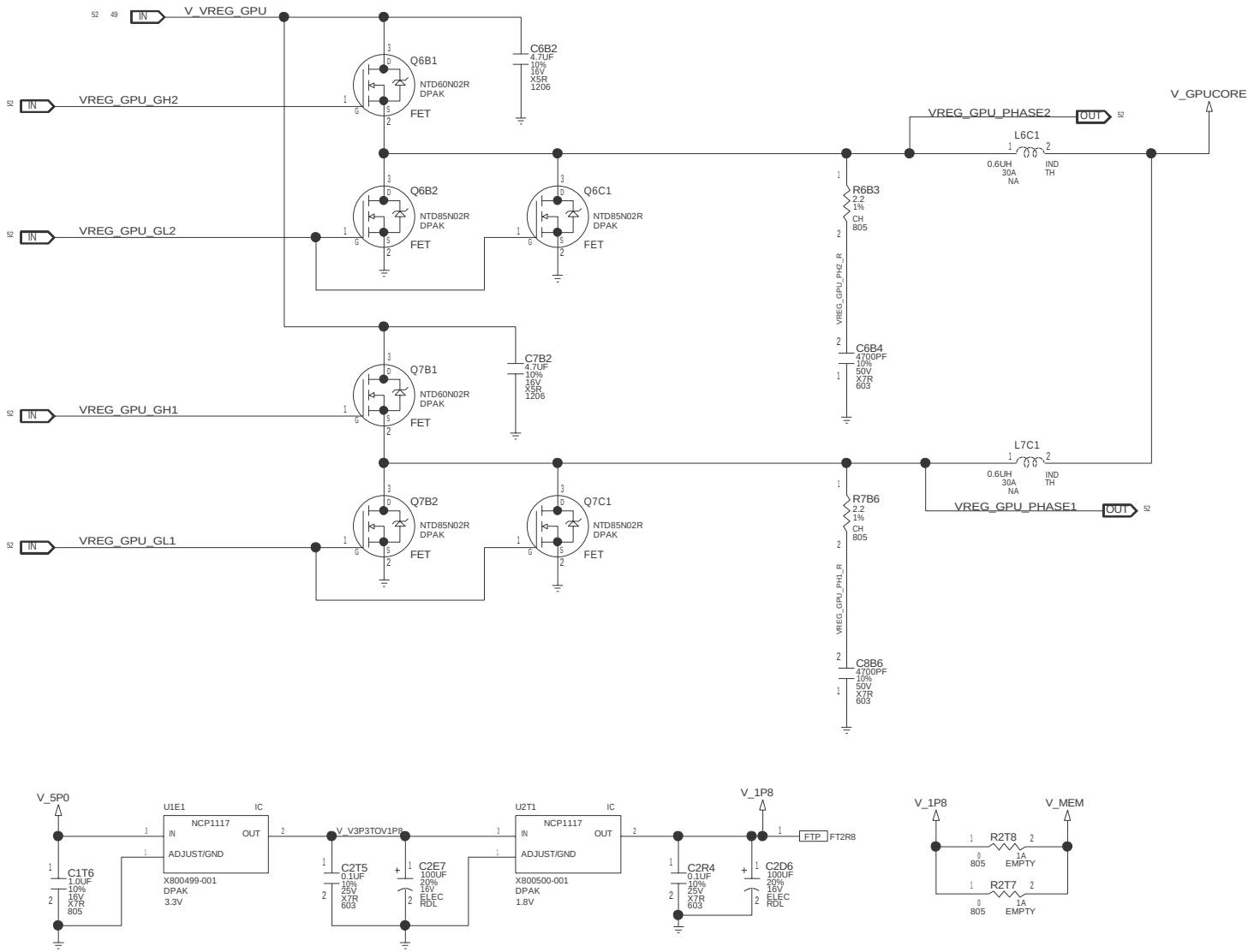
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	51/73	K7



[PAGE_TITLE=VREGS, GPU CONTROLLER]

DRAWING
XENON_FABK
Wed Aug 24 09:27:38 2005

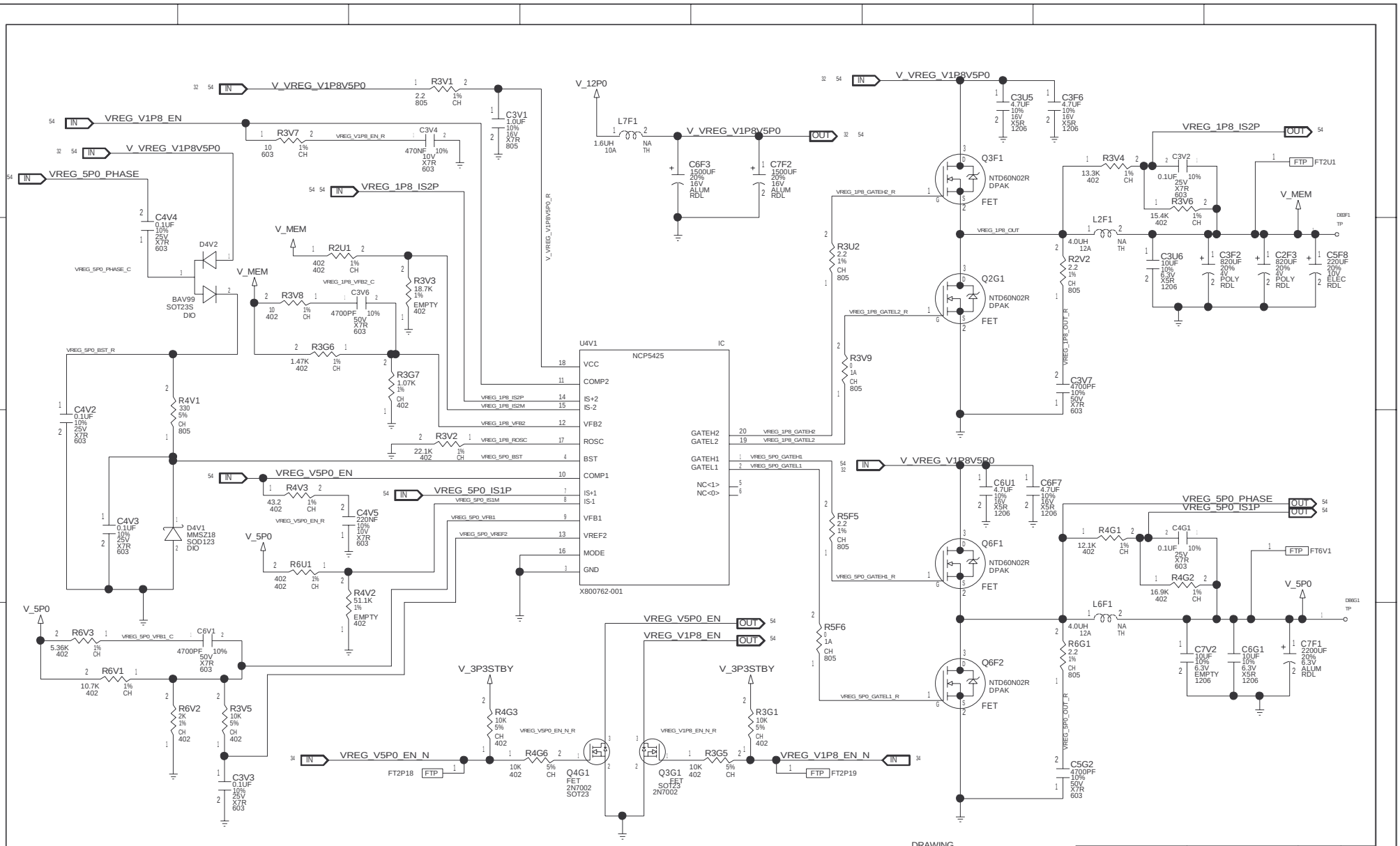
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	52/73	K7



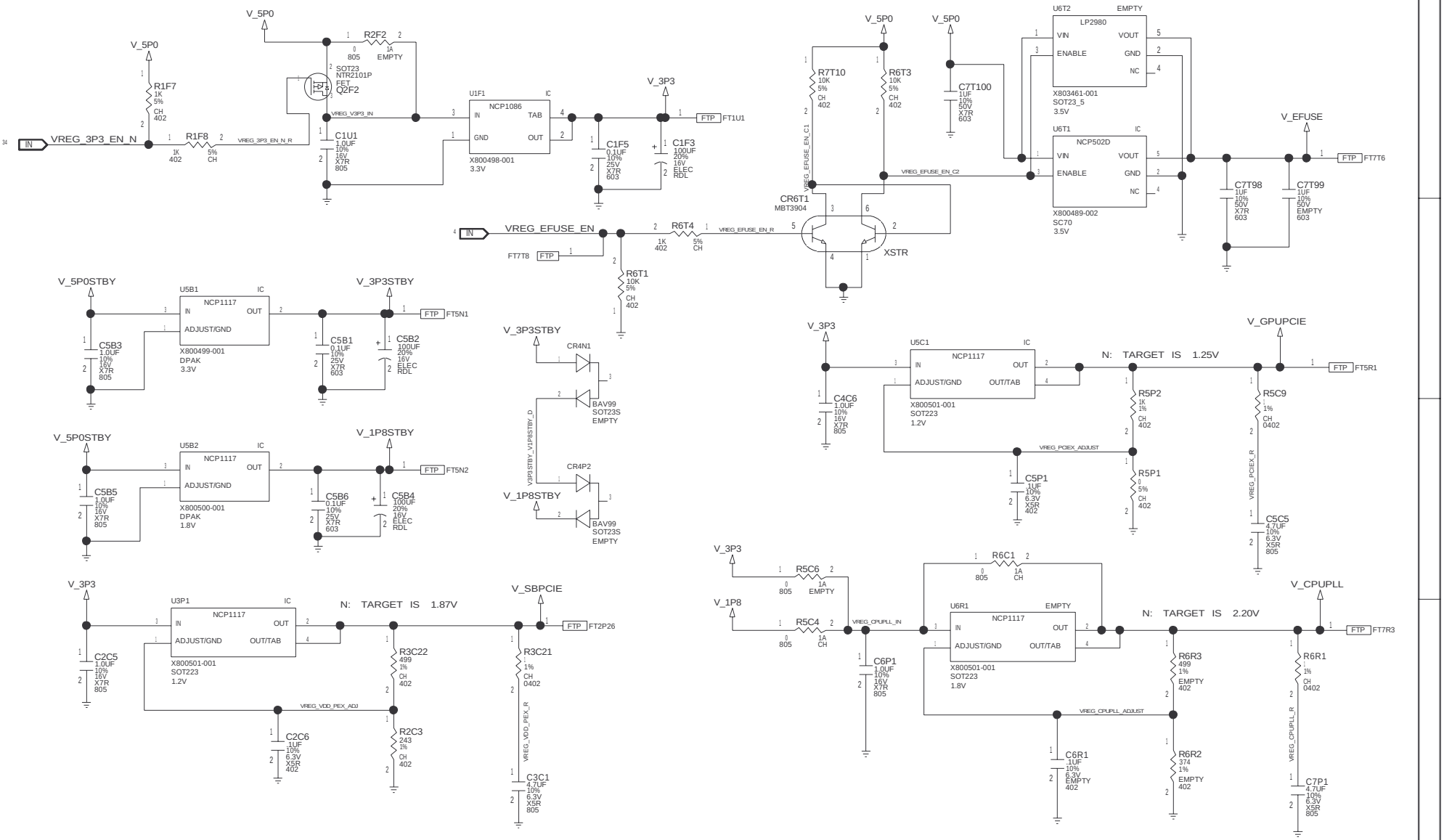
[PAGE_TITLE=VREGS, GPU OUTPUT PHASE 1,2]

DRAWING
XENON_FABK
Wed Aug 24 09:27:39 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	53/73	K7



[PAGE_TITLE=VREGS, V1P8 AND V5P0]

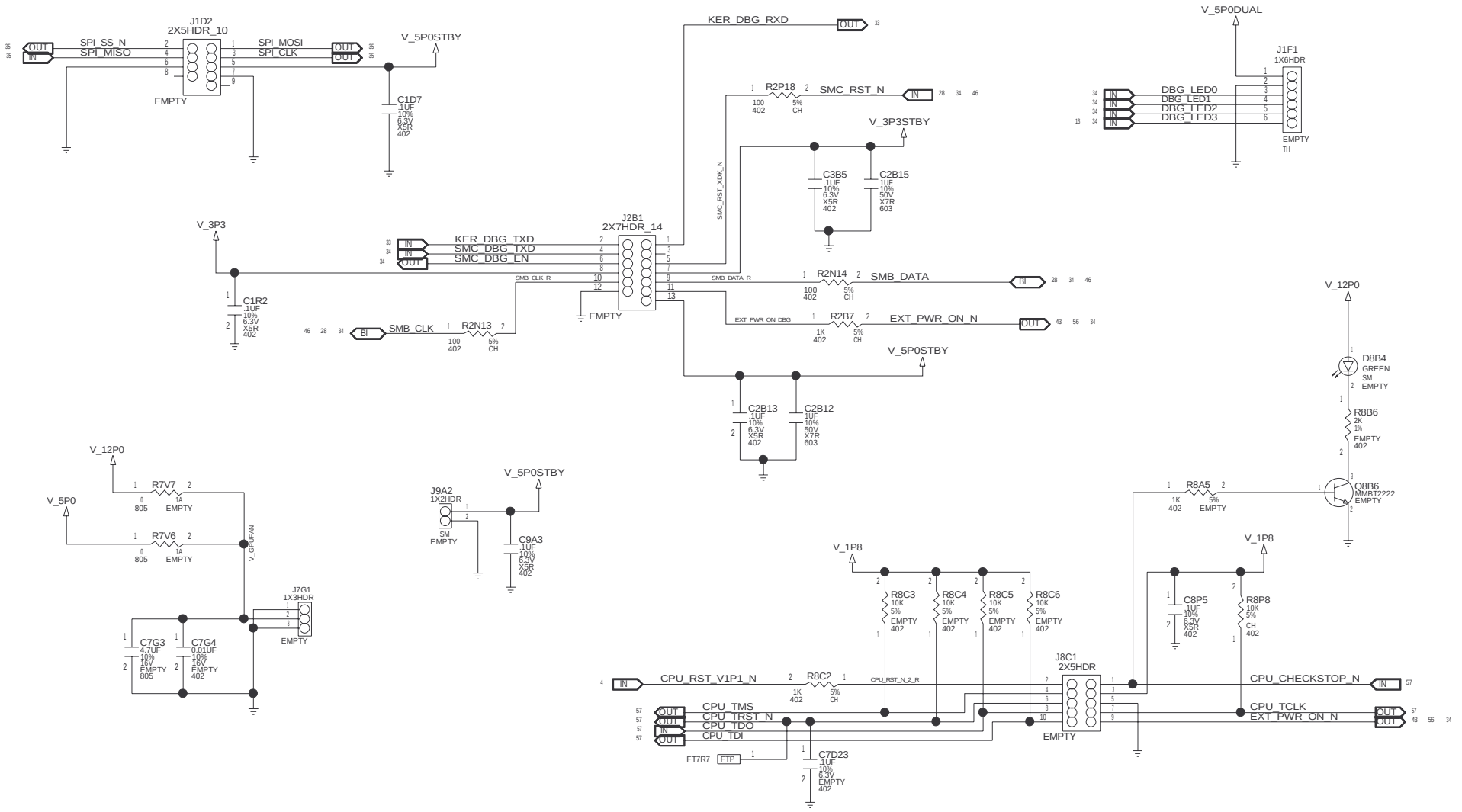


[PAGE_TITLE=[VREGS, LINEAR VREGS]

DRAWING
XENON_FABK
Wed Aug 24 09:27:40 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	55/73	K7

XDK, DEBUG CONNECTORS

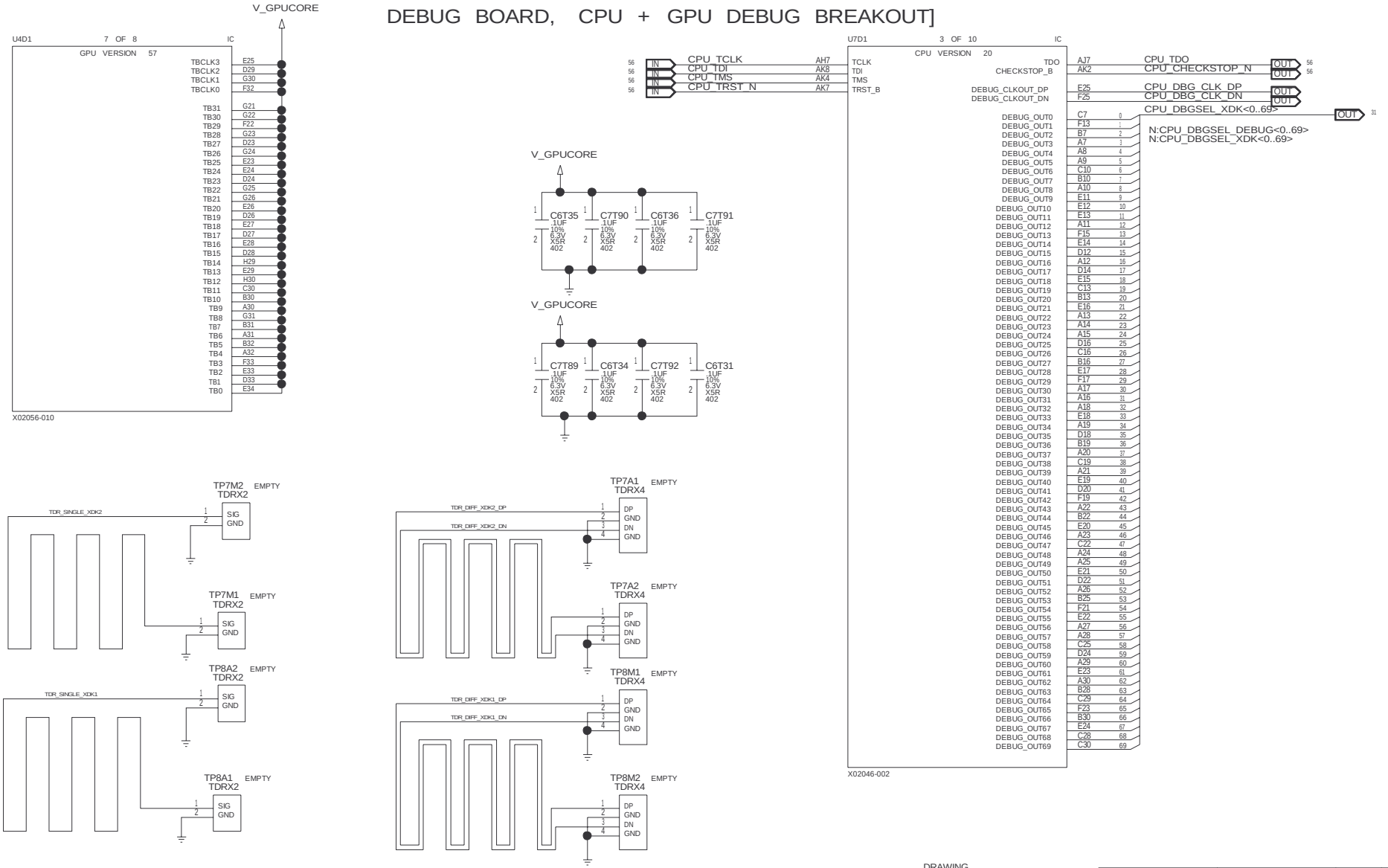


[PAGE_TITLE=XDK. DEBUG CONN]

DRAWING
XENON_FABK
Wed Aug 24 09:26:59 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	56/73	K7

DEBUG BOARD, CPU + GPU DEBUG BREAKOUT]



[PAGE_TITLE=DEBUG BOARD, CPU + GPU DEBUG BREAKOUT]

DRAWING
XENON_FABK
Wed Aug 24 09:27:41 2005

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	REV
	XENON_RETAIL	57/73	K7

INTELLIGENT SERIAL NUMBER TARGET.

LB7G1
LABEL
1375X250_TARGET
X801181-001

WEST PCB MOUNTING HOLES

EDGE
MTG1B1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

EDGE
MTG1G1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

MIDDLE PCB MOUNTING HOLES

CTR
MTG5G1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

CTR
MTG5B1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

EAST PCB MOUNTING HOLES

EDGE
MTG9G1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

EDGE
MTG9B1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

HEAT SINK MOUNTING HOLES

STD
MTG8C1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG3C1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG6C1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG5C1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG6E1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG3E1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG8E1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG5E1
MTG_HOLE
NC9
EMPTY
GND=1,2,3,4,5,6,7,8

*** Signal Cross-Reference for the entire design ***

ANA_CLK_OE 34B3> 28C8< 46B7<
ANA_PIX_CLK_2X_DN 28B1> 13C8<
ANA_PIX_CLK_2X_DP 28B1> 13C8<
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ANA_V12P0_PWRGD 28D3> 34C3< 48A5<
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ANA_VID_INT 29D3> 33B2<
ANA_XTAL_IN 46D2> 28C7<
ARGONPORT_DN 35B4<> 48C8<>
ARGONPORT_DP 35B4<> 48C8<>
ARGON_CLK 34A1<> 48A7<>
ARGON_DATA 34A1<> 48A7<>
ARGON_NTX 48A6> 44B7<
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AUD_CLK 28B1> 36C5<
AUD_L_OUT 40C1> 43B4<
AUD_RST_N 33B2> 40C8<
AUD_R_OUT 40C1> 43B4<
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AV_MODE1 43B1> 34B8< 43A3<
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BRD_TEMP_P 29B1> 29A7<
CAL_TEMP_N 29B1> 29A8<
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CPU_CLK_DP 46D1> 4D6<
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CPU_DBGSEL_XDK<0..69> 57D1> 31D4<
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CPU_DBG_CLK_DP 57D1>
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CPU_FSB_HF_CLKOUT_DP 4C2>
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CPU_SPI_EN 4B2> 4A6<
CPU_SPI_SI 4A1> 4B3> 4B6<
CPU_SPI_SO 4B2> 4A5<
CPU_SPI_WP_N 4A3> 4A2<
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CPU_TDI 56A5> 57D5<
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CPU_TEMP_P 29B1> 4B2<
CPU_TMS 56A5> 57D5<
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DBG_LED1 34B8<> 56D3<
DBG_LED2 34B8<> 56D3<
DBG_LED3 34B8<> 13C7< 56D3<
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DDC_DATA 35B1<> 43C1<>
DDC_DATA_OUT 34C8<> 35B5<>
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EDRAM_TEMP_P 29B1> 13C8<
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ENET_TX_DN 19B3> 39A1<> 44B5<
ENET_TX_DP 19B3> 39C1<> 44B5<
EXPPORT_DN 35B4<> 44C8<>
EXPPORT_DP 35B4<> 44C8<>
EXT_PWR_ON_N 43C1> 56A1> 56C3> 34C8< 43A3<
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FAN1_OUT 29C3> 42D5<
FAN2_FDBK 42A2> 29C6<
FAN2_OUT 29C3> 42B4<
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MA_BA<2..0> 14C5> 20B8< 21B8<
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MA_DQ30 14D8<> 20D5<> 21C5<>
MA_DQ31 14D8<> 20D5<> 21C5<>
MA_RAS_N 14B5> 20B8< 21B8<
MA_RDQS0 20B5> 21B5> 14B8<
MA_RDQS1 20B5> 21B5> 14C8<
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MA_RDQS3 20C5> 21C5> 14D8<
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MA_WDQS3 14D8> 20C5< 21C5<
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MB_A<12..0> 14C1>
MB_BA<2..0> 14C1> 22B8< 23B8<
MB_CAS_N 14B1> 22B8< 23B8<
MB_CKE 14B1> 22B8< 23B8<
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MB_CLK0_DP 14C1> 22D8<
MB_CLK1_DN 14C1> 23C8<
MB_CLK1_DP 14C1> 23D8<
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MB_DM2 14C4> 22C5< 23C5<
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MB_DQ27 14D4<> 22C5<> 23C5<>
MB_DQ28 14D4<> 22C5<> 23C5<>
MB_DQ29 14D4<> 22C5<> 23C5<>
MB_DQ30 14D4<> 22C5<> 23C5<>

MB_DQ31	14D4<>	22D5<>	23C5<>
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MB_RDQS0	22B5>	23B5>	14B4<
MB_RDQS1	22B5>	23B5>	14C4<
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MB_WDQS2	14C4>	22C5<	23C5<
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MB_WE_N	14B1>	22B8<	23B8<
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MC_A<12..0>	15C5>		
MC_BA<2..0>	15C5>	24C8<	25B8<
MC_CAS_N	15B5>	24B8<	25B8<
MC_CKE	15C5>	24B8<	25B8<
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MC_CLK0_DP	15C5>	24D8<	
MC_CLK1_DN	15C5>	25C8<	
MC_CLK1_DP	15D5>	25D8<	
MC_CS0_N	15B5>	24B8<	
MC_CS1_N	15B5>	25B8<	
MC_DM0	15B8>	24B4<	25B4<
MC_DM1	15C8>	24B4<	25B4<
MC_DM2	15C8>	24C4<	25C4<
MC_DM3	15D8>	24C4<	25C4<
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MC_WE_N	15B5>	24B8<	25B8<
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MD_CLK0_DP	15C1>	26D8<	
MD_CLK1_DN	15C1>	27C8<	
MD_CLK1_DP	15D1>	27D8<	

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MD_CS1_N	15B1>	27B8<				
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MD_DM1	15C4>	26B5<	27B5<			
MD_DM2	15C4>	26C5<	27C5<			
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MD_DQ1	15B4<>	26B5<>	27B5<>			
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MD_DQ7	15B4<>	26B5<>	27C5<>			
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MD_DQ9	15C4<>	26B5<>	27B5<>			
MD_DQ10	15C4<>	26B5<>	27B5<>			
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MD_DQ30	15D4<>	26D5<>	27C5<>			
MD_DQ31	15D4<>	26D5<>	27C5<>			
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MD_RDQS2	26C5>	27C5>	15C4<			
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MD_WDQS3	15D4>	26C5<	27C5<			
MD_WE_N	15B1>	26B8<	27B8<			
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MEMPORT1_DP	35C4<>	45B4<>				
MEMPORT2_DN	35B4<>	45C4<>				
MEMPORT2_DP	35B4<>	45C4<>				
MEM_A_VREF0	21A6>	20B8<	21B8<			
MEM_A_VREF1	20A6>	20B8<	21B8<			
MEM_B_VREF0	23A6>	22B8<	23B8<			
MEM_B_VREF1	22A6>	22B8<	23B8<			
MEM_C_VREF0	25A6>	24B8<	25B8<			
MEM_C_VREF1	24A6>	24B8<	25B8<			
MEM_D_VREF0	27A7>	26B8<	27B8<			
MEM_D_VREF1	26A7>	26B8<	27B8<			
MEM_RST	13B3>	20C8<	21C8<	22C8<	23C8<	
	24C8<	25C8<	26C8<	27C8<		
MEM_SCAN_BOT_EN	12A1>	21B8<	23B8<	25B8<	27B8<	
MEM_SCAN_BOT_EN_BUFF	13B3>	12A4<				
MEM_SCAN_EN	12D1>	20B8<	21B8<	22B8<	23B8<	
	24B8<	25B8<	26B8<	27B8<		
MEM_SCAN_EN_BUFF	13B3>	12D4<				
MEM_SCAN_TOP_EN	12B1>	20B8<	22B8<	24B8<	26B8<	
MEM_SCAN_TOP_EN_BUFF	13B3>	12B4<				
MII_COL	19B6>	39B7>	36C6<			
MII_CRS	19B6>	39B7>	36C6<			
MII_MDC_CLK_OUT	36D2>	19B6<	39C8<			
MII_MDIO	19B6<>	36C6<>	39B8<>			
MII_RXD0	19B7>	39C7>	36C6<			
MII_RXD1	19B6>	39C7>	36C6<			
MII_RXD2	19B6>	39C7>	36C6<			
MII_RXD3	19C6>	39C7>	36C6<			

MII_RXDV	19C6>	39C7>	36C6<			
MII_RXER	19C6>	39C7>	36C6<			
MII_RX_CLK	19C6>	39C7>	36D7<			
MII_TXD0	36C3>	19B6<	39B7<			
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MII_TXD2	36C3>	19B6<	39B7<			
MII_TXD3	36C3>	19B6<	39C7<			
MII_TXEN	36C3>	19B6<	39C7<			
MII_TX_CLK	19B6>	39C7>	36D7<			
ODD_RX_DN	47A8>	36B6<				
ODD_RX_DP	47A8>	36B6<				
ODD_TX_DN	36B3>	47A8<				
ODD_TX_DP	36B3>	47B8<				
PCIEX_CLK_DN	46B1>	33C6<				
PCIEX_CLK_DP	46B1>	33C6<				
PEX_GPU_SB_L0_DN	13C1>	33C7<				
PEX_GPU_SB_L0_DP	13D1>	33C7<				
PEX_GPU_SB_L1_DN	13D1>	33C7<				
PEX_GPU_SB_L1_DP	13D1>	33C7<				
PEX_SB_GPU_L0_DN	33C1>	13D8<				
PEX_SB_GPU_L0_DP	33C1>	13D8<				
PEX_SB_GPU_L1_DN	33D1>	13D8<				
PEX_SB_GPU_L1_DP	33D1>	13D8<				
PIX_DATA<14..0>	13C3>	29D6<				
PSU_V12P0_EN	34B3>	48C5<				
PWRSW_N	34C3>	48B8<				
SATA_CLK_DN	46B1>	33D6<				
SATA_CLK_DP	46B1>	33D6<				
SATA_CLK_REF	46A1>	33D6<				
SB_GPIO<0..15>	33B1<>	33B5<>				
SB_MAIN_PWRGD	34B1>	34C6<				
SB_RST_N	34B3>	34C6<				
SCART_RGB	33B2>	43A6<				
SMB_CLK	34B8<>	56C7<>	28B6<	46B6<		
SMB_DATA	28B7<>	34B8<>	56C3<>	46B6<		
SMC_DBG_EN	56C6>	34C6<				
SMC_DBG_TXD	34C3>	56C6<				
SMC_PWM0	34B3>	29B8<				
SMC_PWM1	34B3>	29C8<				
SMC_RST_N	28D3>	34D6<	46C8<	56D3<		
SPDIF	36C1>	43D6<				
SPI_CLK	56D6>	35D7<				
SPI_MISO	35D3>	56D8<				
SPI_MOSI	56D6>	35D7<				
SPI_SS_N	56D8>	35D7<				
STBY_CLK	46A1>	34D6<				
TILTSW_N	42B6>	34B3<				
TRAY_OPEN	34D8>	47A1<				
TRAY_STATUS	47A4>	34C6<				
VID_DACA_DP	29D3>	43D8<				
VID_DACA_OUT	43D5>	43C4<				
VID_DACB_DP	29D3>	43C8<				
VID_DACB_OUT	43C6>	43C4<				
VID_DACC_DP	29D3>	43C8<				
VID_DACC_OUT	43C6>	43C4<				
VID_DACD_DP	29D3>	43B8<				
VID_DACD_OUT	43B6>	43B4<				
VID_HSYNC_OUT	43A4>	43B4<				
VID_HSYNC_OUT_R	29C3>	43A7<				
VID_VSYNC_OUT	43A6>	43B4<				
VID_VSYNC_OUT_R	29C3>	43A8<				
VREG_1P8_IS2P	54D1>	54D7<	54D7<			
VREG_3P3_EN_N	34C3>	55D8<				
VREG_5P0_IS1P	54B1>	54B6<				
VREG_5P0_PHASE	54B1>	54D8<				
VREG_CPU_DRV_EN	50C1>	51D8<				
VREG_CPU_EN	34B3>	50D7<				
VREG_CPU_PHASE1	51A1>	50C8<				
VREG_CPU_PHASE2	51C1>	50C8<				
VREG_CPU_PHASE3	51D1>	50C8<				
VREG_CPU_PWM1	50C2>	51A7<				
VREG_CPU_PWM2	50C2>	51B7<				
VREG_CPU_PWM3	50C2>	51D7<				
VREG_CPU_PWRGD	50C2>	34C1<				
VREG_CPU_VID<5..0>	49C2>	50C2<				
VREG_EFUSE_EN	4D2>	55C6<				
VREG_GPU_5VREF	52C3>	52C6<				

VREG_GPU_EN_N	34C3>	52B3<				
VREG_GPU_GH1	52A1>	53C7<				
VREG_GPU_GH2	52A1>	53D7<				
VREG_GPU_GL1	52A1>	53B7<				
VREG_GPU_GL2	52A1>	53C7<				
VREG_GPU_PHASE1	52D1>	53B2>	52B8<			
VREG_GPU_PHASE2	53D2>	52B8<				
VREG_GPU_PWRGD	52A1>	34D1<				
VREG_V1P8_EN	54A4>	54D8<				
VREG_V1P8_EN_N	34B3>	54A3<				
VREG_V5P0_EN	54A4>	54B7<				
VREG_V5P0_EN_N	34B3>	54A7<				
VREG_V5P0_SEL	34B3>	46A8<				
V_CMPAVDD33_USB	37A7>	37C2<				
V_ENET	39A3>	19C3<	19C7<	39B8<	39B8<	
	39D5<	44B6<				
V_EXPPORT	44B7<	44D4	44D7<			
V_MEMPORT1	45D1>					
V_VREG_CPU	49B4>	50D7<	51D5<	51D8<		
V_VREG_GPU	49B1>	52D4<	52D7<	53D7<		
V_VREG_V1P8V5P0	54D4>	32D4<	54B4<	54D4<	54D7<	
	54D8<					
WSS_CNTL0	33B2>	43B6<				
WSS_CNTL1	33B2>	43B6<				

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*** Part Cross-Reference for the entire design ***

C1A2	CAPN	44
C1A3	CAPN	44
C1A4	CAPN	44
C1A5	CAP_P	39
C1B1	CAPN	39
C1B2	CAPN	32
C1B3	CAPN	32
C1B4	CAPN	28
C1C1	CAPN	32
C1C2	CAPN	33
C1C3	CAPN	47
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C1C6	CAPN	47
C1C7	CAPN	32
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C1C9	CAPN	36
C1C10	CAP_P	47
C1C11	CAP_P	47
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C1D8	CAPN	32
C1D9	CAP_P	47
C1D10	CAPN	32
C1D11	CAP_P	46
C1E1	CAPN	47
C1E2	CAPN	47
C1E3	CAPN	47
C1E4	CAPN	47
C1E5	CAP_P	47
C1F1	CAPN	32
C1F2	CAPN	32
C1F3	CAP_P	55
C1F4	CAP_P	45
C1F5	CAPN	55
C1F6	CAPN	45
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C1M2	CAPN	44
C1N1	CAPN	39
C1N2	CAPN	39
C1N3	CAPN	39
C1N4	CAPN	39
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C2A2	CAPN	43
C2A3	CAPN	43
C2A4	CAP_P	44
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C2A6	CAPN	43
C2A7	CAPN	40
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C2D2	CAPN	26
C2D3	CAPN	24
C2D4	CAPN	26
C2D5	CAPN	12
C2D6	CAP_P	53
C2E1	CAPN	24
C2E2	CAPN	26
C2E3	CAPN	24
C2E4	CAPN	12
C2E5	CAPN	41
C2E6	CAPN	41
C2E7	CAP_P	53
C2E8	CAPN	24
C2F2	CAPN	32
C2F3	CAP_P	54
C2G1	CAPN	32
C2G2	CAP_P	45
C2G3	CAPN	45
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C2R11	CAPN	41
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C9U1	CAPN	51
C9U2	CAPN	51
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C9V3	CAPN	45
CR1D1	MBT3904DUAL	46
CR1D2	DIOSOT23S	47
CR1D3	DIOSOT23S	47
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CR2N1	MBT3904DUAL	40
CR4N1	DIOSOT23S	55
CR4P2	DIOSOT23S	55
CR6T1	MBT3904DUAL	55
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D1A2	DIOSOT23S	44
D1B1	DIOSOT23S	44
D1E1	DIOSOT23S	47
D1E2	DIOSOT23S	47
D1E3	DIOSOT23S	47
D1E4	DIOSOT23S	47
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D2A2	DIOSOT23S	43
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D2M3	DIOSOT23S	35
D3A1	DIODE	42
D3A2	DIOSOT23S	43
D3A3	DIOSOT23S	43
D3A4	DIOSOT23S	43
D3B1	DIODE	42
D3M2	DIOSOT23S	43
D3M3	DIOSOT23S	43
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D8B2	DIODE	52
D8B3	DIOSOT23S	52
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D9C1	DIODE	51
D9E1	DIODE	51
D9F1	DIODE	51
D9G1	DIOSOT23S	45
D9G2	DIOSOT23S	45
D9V1	DIOSOT23S	45
D9V2	DIOSOT23S	45

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DB8M2	DBPAD	48
DB8M3	DBPAD	48
DB8P1	DBPAD	49
DB8P2	DBPAD	49
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EG1A2	ESDGUARD	44
EG1E1	ESDGUARD	47
EG1E2	ESDGUARD	47
EG1E3	ESDGUARD	47
EG1E4	ESDGUARD	47
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EG9V1	ESDGUARD	45
EG9V2	ESDGUARD	45
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FB1N1	FERRITE	19
FB1P1	FERRITE	38
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FB1P3	FERRITE	38
FB1P4	FERRITE	38

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FB2A2	FERRITE	40
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FB3P1	FERRITE	46
FB3P2	FERRITE	46
FB4C2	FERRITE	30
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FB4N3	FERRITE	30
FB4N4	FERRITE	30
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FT7T7	FTPAD	4
FT7T8	FTPAD	55
FT7U1	FTPAD	49
FT8N1	FTPAD	48
FT9N1	FTPAD	48
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J1C1	1X7SATA	47
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J1D2	2X5HDR10	56
J1E1	XENONHDD	47
J1F1	1X6HDR	56
J2A1	XENONAVIP	43
J2B1	2X7HDR14	56
J2D1	2X3HDR	33
J2D2	2X4HDR	13
J3A1	2X2HDR	42
J3G1	XENONMU	45
J5C1	2X3HDR	28
J5C2	2X3HDR	13
J6G1	XENONRF	48
J7F1	2X3HDR	4
J7G1	1X3HDR	56
J8C1	2X5HDR	56
J9A1	XENONPWR	48
J9A2	1X2HDR	56
J9G1	XENONGAME	45
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L2A1	INDUCTOR	43
L2F1	INDUCTOR	54
L2G1	CMCHOKE	45
L3A1	INDUCTOR	43
L3A2	INDUCTOR	43
L3A3	INDUCTOR	43
L4G1	CMCHOKE	45
L6C1	INDUCTOR	53
L6F1	INDUCTOR	54
L6G1	CMCHOKE	48
L7C1	INDUCTOR	53
L7F1	INDUCTOR	54
L8B1	INDUCTOR	49
L8D1	INDUCTOR	51
L8E1	INDUCTOR	51
L8F1	INDUCTOR	51
L9B1	INDUCTOR	49
L9G1	CMCHOKE	45
L9V1	CMCHOKE	45
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MTG1G1	STD_MTG_HOLE	58
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MTG3E1	STD_MTG_HOLE	58
MTG5B1	STD_MTG_HOLE	58
MTG5C1	STD_MTG_HOLE	58
MTG5E1	STD_MTG_HOLE	58
MTG5G1	STD_MTG_HOLE	58
MTG6C1	STD_MTG_HOLE	58
MTG6E1	STD_MTG_HOLE	58
MTG8C1	STD_MTG_HOLE	58
MTG8E1	STD_MTG_HOLE	58
MTG9B1	STD_MTG_HOLE	58
MTG9G1	STD_MTG_HOLE	58
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Q1G2	NPN	46
Q1G3	PNP	29
Q1V1	NPN	46
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Q2G1	FET_VREG	54
Q2M1	PNP	43
Q2N1	PNP	40
Q2N2	NPN	35
Q3A1	NPN	42
Q3A2	PNP_2C	42
Q3F1	FET_VREG	54
Q3G1	FET	54
Q3M1	PNP_2C	42
Q3M4	NPN	42
Q4G1	FET	54
Q6B1	FET_VREG	53
Q6B2	FET_VREG	53
Q6C1	FET_VREG	53
Q6F1	FET_VREG	54
Q6F2	FET_VREG	54
Q7B1	FET_VREG	53
Q7B2	FET_VREG	53
Q7C1	FET_VREG	53
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Q8F1	FET_VREG	51
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R5D2	RESN	13
R5E1	RESN	14
R5E2	RESN	14
R5F1	RESN	23
R5F2	RESN	23
R5F3	RESN	22
R5F4	RESN	22
R5F5	RESN	54
R5F6	RESN	54
R5N1	RESN	52
R5P1	RESN	55
R5P2	RESN	55
R5P3	RESN	13
R5R1	RESN	12
R5R2	RESN	12
R5R3	RESN	12
R5U1	RESN	23
R5U2	RESN	23
R5U3	RESN	22
R5U4	RESN	22
R5V2	RESN	42
R5V3	RESN	42
R6B3	RESN	53
R6C1	RESN	55
R6D1	RESN	4
R6D2	RESN	4
R6E1	RESN	4
R6E2	RESN	4
R6G1	RESN	54
R6G7	RESN	48
R6G8	RESN	48
R6R1	RESN	55
R6R2	RESN	55
R6R3	RESN	55
R6R4	RESN	4
R6R5	RESN	4
R6R6	RESN	4
R6R7	RESN	4
R6R8	RESN	4
R6R9	RESN	4
R6R10	RESN	4
R6T1	RESN	55
R6T3	RESN	55
R6T4	RESN	55
R6U1	RESN	54
R6V1	RESN	54
R6V2	RESN	54
R6V3	RESN	54
R7B2	RESN	48
R7B6	RESN	53
R7D1	RESN	4
R7E1	RESN	49
R7E2	RESN	49
R7E3	RESN	49
R7E4	RESN	49
R7E5	RESN	49

R7E6	RESN	49
R7E7	RESN	4
R7E8	RESN	4
R7F1	RESN	4
R7F2	RESN	4
R7F3	RESN	4
R7F4	RESN	4
R7F5	RESN	50
R7F7	RESN	4
R7N1	RESN	48
R7N2	RESN	48
R7N3	RESN	48
R7N4	RESN	48
R7R1	RESN	4
R7R2	RESN	4
R7R3	RESN	4
R7R4	RESN	4
R7R5	RESN	4
R7R6	RESN	4
R7R7	RESN	4
R7R8	RESN	4
R7R9	RESN	4
R7R10	RESN	4
R7R11	RESN	4
R7R12	RESN	4
R7R13	RESN	4
R7R14	RESN	4
R7R15	RESN	4
R7R16	RESN	4
R7R17	RESN	4
R7R18	RESN	4
R7R19	RESN	4
R7R20	RESN	4
R7R21	RESN	4
R7R22	RESN	4
R7R23	RESN	4
R7R24	RESN	4
R7T2	RESN	6
R7T4	RESN	49
R7T5	RESN	49
R7T6	RESN	49
R7T7	RESN	49
R7T8	RESN	49
R7T9	RESN	49
R7T10	RESN	55
R7T11	RESN	49
R7T12	RESN	49
R7T13	RESN	49
R7T14	RESN	49
R7T15	RESN	49
R7T16	RESN	49
R7U1	RESN	50
R7U2	RESN	50
R7U3	RESN	4
R7V1	RESN	50
R7V2	RESN	50
R7V3	RESN	50
R7V4	RESN	34
R7V5	RESN	50
R7V6	RESN	56
R7V7	RESN	56
R8A1	RESN	48
R8A2	RESN	48
R8A3	RESN	48
R8A4	RESN	48
R8A5	RESN	56
R8B2	RESN	52
R8B3	RESN	52
R8B4	RESN	52
R8B5	RESN	48
R8B6	RESN	56
R8C1	RESN	52
R8C2	RESN	56
R8C3	RESN	56
R8C4	RESN	56
R8C5	RESN	56
R8C6	RESN	56

R8G3	RESN	50
R8N1	RESN	48
R8N2	RESN	52
R8N3	RESN	52
R8N4	RESN	52
R8N5	RESN	52
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R8N7	RESN	52
R8N8	RESN	52
R8N9	RESN	52
R8N10	RESN	52
R8N11	RESN	52
R8N12	RESN	52
R8N17	RESN	34
R8N18	RESN	34
R8P1	RESN	52
R8P2	RESN	52
R8P3	RESN	52
R8P4	RESN	52
R8P5	RESN	52
R8P6	RESN	52
R8P7	RESN	52
R8P8	RESN	56
R8P9	RESN	52
R8U1	RESN	50
R8U2	RESN	50
R8U3	RESN	50
R8U4	RESN	50
R8V1	RESN	50
R8V2	RESN	50
R8V3	RESN	50
R8V4	RESN	50
R8V5	RESN	50
R9B1	RESN	52
R9C1	RESN	51
R9E1	RESN	51
R9F1	RESN	51
R9G1	RESN	45
R9G2	RESN	45
R9P1	RESN	51
R9P2	RESN	51
R9T1	RESN	51
R9T2	RESN	51
R9U1	RESN	51
R9U2	RESN	51
R9V1	RESN	45
R9V2	RESN	45
RT1B1	THERMISTOR	44
RT1R1	THERMISTOR	47
RT1U1	THERMISTOR	47
RT2G1	THERMISTOR	45
RT2M1	THERMISTOR	43
RT7C1	THERMISTOR	52
RT8F1	THERMISTOR	50
RT8G1	THERMISTOR	45
RT8G2	THERMISTOR	45
ST1P1	SHORT	38
ST1P2	SHORT	38
ST1P3	SHORT	38
ST2P1	SHORT	38
ST2P2	SHORT	37
ST2P3	SHORT	37
ST2P4	SHORT	37
ST4C1	SHORT	29
ST4C2	SHORT	29
ST4C3	SHORT	29
ST4C4	SHORT	29
ST4C5	SHORT	29
ST5D1	SHORT	52
ST5R1	SHORT	52
ST5R2	SHORT	52
ST6D1	SHORT	6
ST6R1	SHORT	6
ST6R2	SHORT	6
ST7D1	SHORT	6
ST7R1	SHORT	6
ST7T1	SHORT	50

ST8F1	SHORT	50
SW1G1	SWITCH	42
SW2G1	SWITCH	42
SW2G2	SWITCH	42
SW5G1	SWITCH	42
TP6D1	PROBE	4
TP6R1	PROBE	4
TP6R2	PROBE	4
TP7A1	TDRX4	57
TP7A2	TDRX4	57
TP7M1	TDRX2	57
TP7M2	TDRX2	57
TP7R1	PROBE	4
TP7R2	PROBE	4
TP7R3	PROBE	4
TP7R4	PROBE	4
TP8A1	TDRX2	57
TP8A2	TDRX2	57
TP8M1	TDRX4	57
TP8M2	TDRX4	57
U1B1	BCM5241	19
U1B2	ICS1893BF	39
U1E1	NCP1117	53
U1F1	NCP1086	55
U1F2	NCP1117	45
U1G1	IR_WHOLDER	42
U1R1	SI4501DY	46
U2B1	XDAC	40
U2C1	SB	33 34 35 36 37 38
U2D1	SN74LVC1G125	12
U2E1	NAND	41
U2E2	SN74LVC1G125	12
U2R1	SN74LVC1G125	12
U2T1	NCP1117	53
U3B4	MK1493REV13	46
U3D1	GDDR136	24
U3E1	GDDR136	26
U3P1	NCP1117	55
U3R1	GDDR136	25
U3T1	GDDR136	27
U4B1	ANA	28 29 30
U4C1	AT25020A	13
U4D1	NB	12 13 14 15 16 17 57
U4F1	GDDR136	20
U4U1	GDDR136	21
U4V1	NCP5425	54
U5B1	NCP1117	55
U5B2	NCP1117	55
U5C1	NCP1117	55
U5F1	GDDR136	22
U5U1	GDDR136	23
U6R1	NCP1117	55
U6T1	NCP502D	55
U6T2	LP2980	55
U7D1	WATERNOOSE	4 5 6 7 8 57
U7E1	AT25020A	4
U7U1	ADP3188	50
U8N1	NCP5331	52
U8P1	MOSDRIVER	51
U9T1	MOSDRIVER	51
U9U1	MOSDRIVER	51
Y3B1	CRYSTAL	46