

REV	DESCRIPTION	DATE	BY
0	ENGINEERING PROTOTYPE	10/06/81	CR
0	DEVELOPER/WORK IN PROGRESS RELEASE	11/06/81	CR
1	ADVANCE ENGINEERING RELEASE	1/15/82	CR
2	REVISED PER ECO 930008	3/27/82	CR
A	PILOT PRODUCTION RELEASE	4/15/82	CR
A	REVISED PER ECO 930162	7-2-82	CR
C	REVISED PER ECO 930177 (M)	7-17-82	CR
D	REVISED PER ECO 930222	8-11-82	CR
E	REVISED		

WC 3267

7/15/93

### SIGNAL GLOSSARY

SIGNAL	DESCRIPTION (AREA)	PAGES
20MHZ	20.53636 MHZ MASTER CLOCK	
7MHZ	7.15909 MHZ PROCESSOR CLOCK	
A(23:1)	PROCESSOR ADDRESS BUS (60000)	
ACK	DATA ACKNOWLEDGE (PARALLEL PORT)	
AS	ADDRESS STROBE (60000)	
AUDIIN	AUDIO INPUT (RS232 PORT)	
AUDIOOUT	AUDIO OUTPUT (RS232 JACK)	
BEER	BUS ERROR (60000)	
BS	BUS STANDBY (60000)	
BSACK	BUS STANDBY ACKNOWLEDGE (60000)	
CLISS	CLITTER SLOWDOWN (CHIPS)	
CLL	CHIP MEMORY ACCESS (CHIPS)	
CR	CPU REQUEST (60000)	
DVSI	DEVICE BUSY (PARALLEL PORT)	
CSA1/2/3	COLUMN ADDRESS STROBE (URAM)	
CC/CCRO	COLOR LOCK / QUADRATURE (CHIPS)	
CDAC	7.15909 MHZ QUADRATURE CLOCK (CHIPS)	
CHNO	MEDIA CHANGE (FLOPPY)	
CLKRD/WR	CLOCK READ / WRITE (RISC)	
COMP	COMPOSITE VIDEO (VIDEO)	
CSYNC	COMPOSITE SYNC (VIDEO)	
CLS	CLEAR TO SEND (RS232 PORT)	
D(15:0)	PROCESSOR DATA BUS (60000)	
DIA	DISK DISJECTION (FLOPPY)	
DISRD	DISK READ DATA (FLOPPY)	
DISWR	DISK WRITE DATA (FLOPPY)	
DMR	DISK WRITE ENABLE (FLOPPY)	
DHAL	CHIP DMA REQUEST LINE (CHIPS)	
URAL(0)	URAM ADDRESS BUS (URAM)	
URAL(15:0)	URAM DATA BUS (URAM)	
USR	DATA SET READY (RS232 PORT)	
DTACK	DATA TRANSFER ACKNOWLEDGE (60000)	
DTR	DATA TERMINAL READY (RS232 PORT)	
E	PERIPHERAL ENABLE CLOCK (60000)	
EXTICK	EXPANSION PRESENT / RIC TICK	
F(12:0)	FUNCTION CODE (60000)	
FIRE(0/1)	FIRE BUTTON Q/L (JOYSTICKS)	
H(1)	PROCESSOR HALT (60000)	
H SYNC	HORIZONTAL SYNC (VIDEO)	
INTRK	INPUT PULSE (FLOPPY)	
INT(2:3,6)	INTERRUPT REQUEST (CHIPS)	
IORESET	I/O RESET	
IPL(2:0)	INTERRUPT PRIORITY LEVEL (60000)	
KDLOCK	KEYBOARD CLOCK (KEYBOARD)	
KDDATA	KEYBOARD DATA (KEYBOARD)	
KDRESET	KEYBOARD RESET (KEYBOARD)	
LUS/DUS	UPPER / LOWER DATA STROBES (60000)	
LED	POWER ON LED / AUDIO FILTER DISABLE	
LEFT/RIGHT	LEFT / RIGHT AUDIO (AUDIO)	

SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	LIGHT PEN TRIGGER (JOYSTICKS)	
MIO	MONITOR ON (FLOPPY)	
MIRO	MONITOR ON - DRIVE 0 (FLOPPY)	
MOY/MIH	MOUSE 0 QUADRATURE V/H (JOYSTICKS)	
MIV/MIH	MOUSE 1 QUADRATURE V/H (JOYSTICKS)	
OVL	OVERLAY AND OVER BAR	
OVR	OVERRIDE SYSTEM DECODING	
PIXELSW	DEBLOCK PIXEL SWITCH (VIDEO)	
POD0/0Y	POI LINES 0 X/Y (JOYSTICKS)	
POI1X/1Y	POI LINES 1 X/Y (JOYSTICKS)	
POI	PAPER OUT (PARALLEL PORT)	
PCD(7:0)	PARALLEL PORT DATA (PARALLEL PORT)	
RDEN	RAM ENABLE (CHIPS)	
RDPEN	CHIP REGISTER ENABLE (CHIPS)	
RAS(0/1)	ROW ADDRESS STROBE (URAM)	
RDY	DRIVE READY (FLOPPY)	
RESET	GENERAL RESET	
RAS(3:1)	REGISTER ADDRESS BUS (CHIPS)	
R/O/D	READ / WRITE / DRIVE (VIDEO)	
RI	RING INDICATOR (RS232 PORT)	
RDEN	RAM ENABLE (ROM)	
RIS	REQUEST TO SEND (RS232 PORT)	
RSI	PROCESSOR RESET (60000)	
RWD	RECEIVE DATA (RS232 PORT)	
RW	PROCESSOR READ/WRITE (60000)	
SEL	SELECT (PARALLEL PORT)	
SEL(3:0)	DRIVE SELECT (FLOPPY)	
SIDE	SIDE SELECT (FLOPPY)	
SILP	SILENCE IN/OUT (COMMAND FLOPPY)	
IRKU	IRACK Z/LNO SENSE (FLOPPY)	
IRKO	IRACKSHUT DATA (RS232 PORT)	
VHM	VALID MEMORY ADDRESS (60000)	
VPA	VALID PERIPHERAL ADDRESS (60000)	
VSYNC	VERTICAL SYNC (VIDEO)	
WE	WRITE ENABLE (URAM)	
WPROT	WRITE PROTECT SENSE (FLOPPY)	
XCLK	EXTERNAL DEBLOCK CLOCK (VIDEO)	
XCLKEN	EXTERNAL CLOCK ENABLE (VIDEO)	
XRDY	EXTERNAL DATA READY	
** CIRCUIT BOARD AND I/O STUFF **		

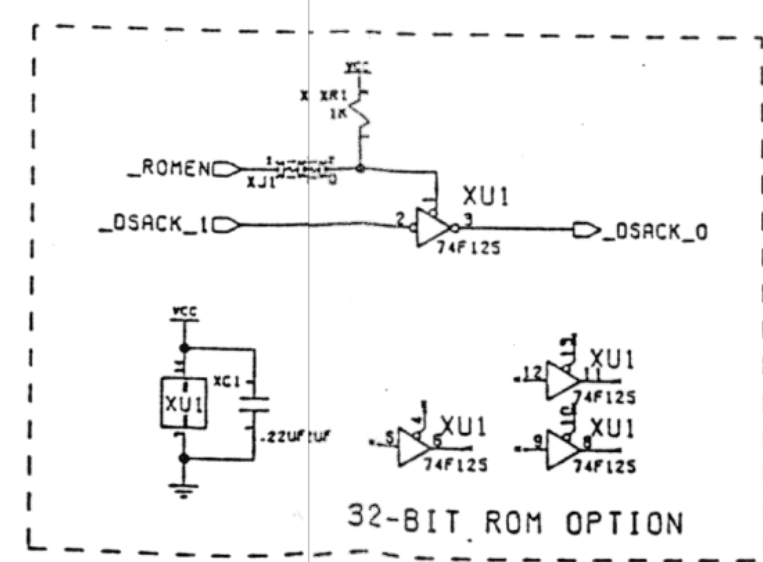
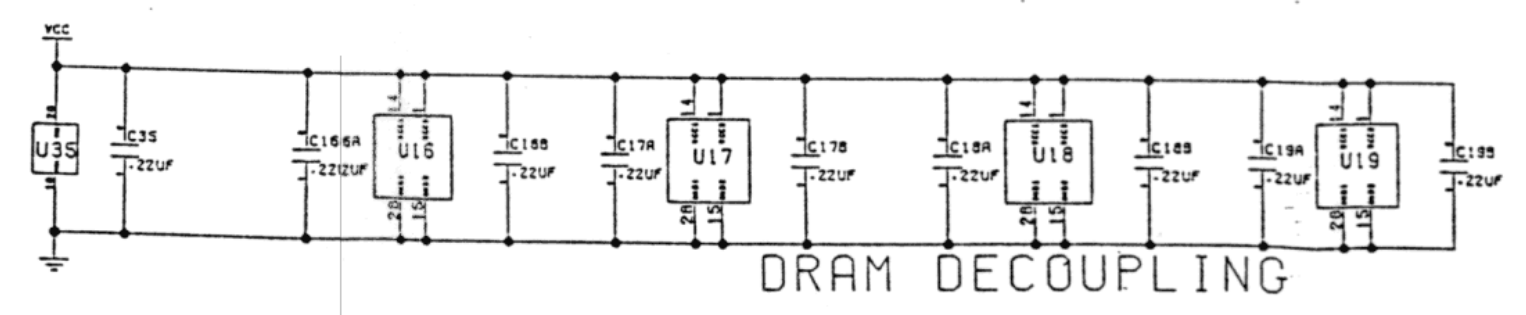
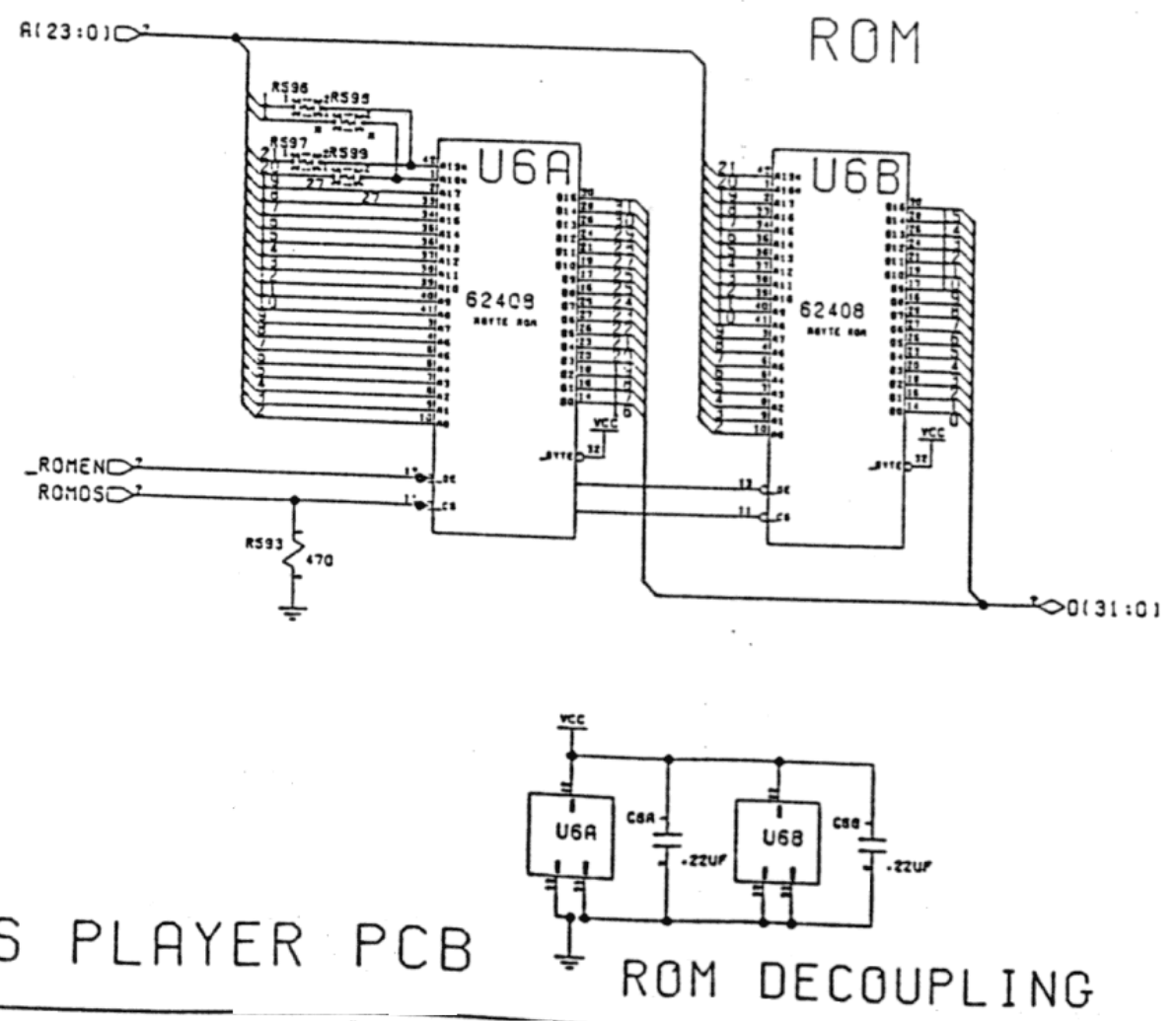
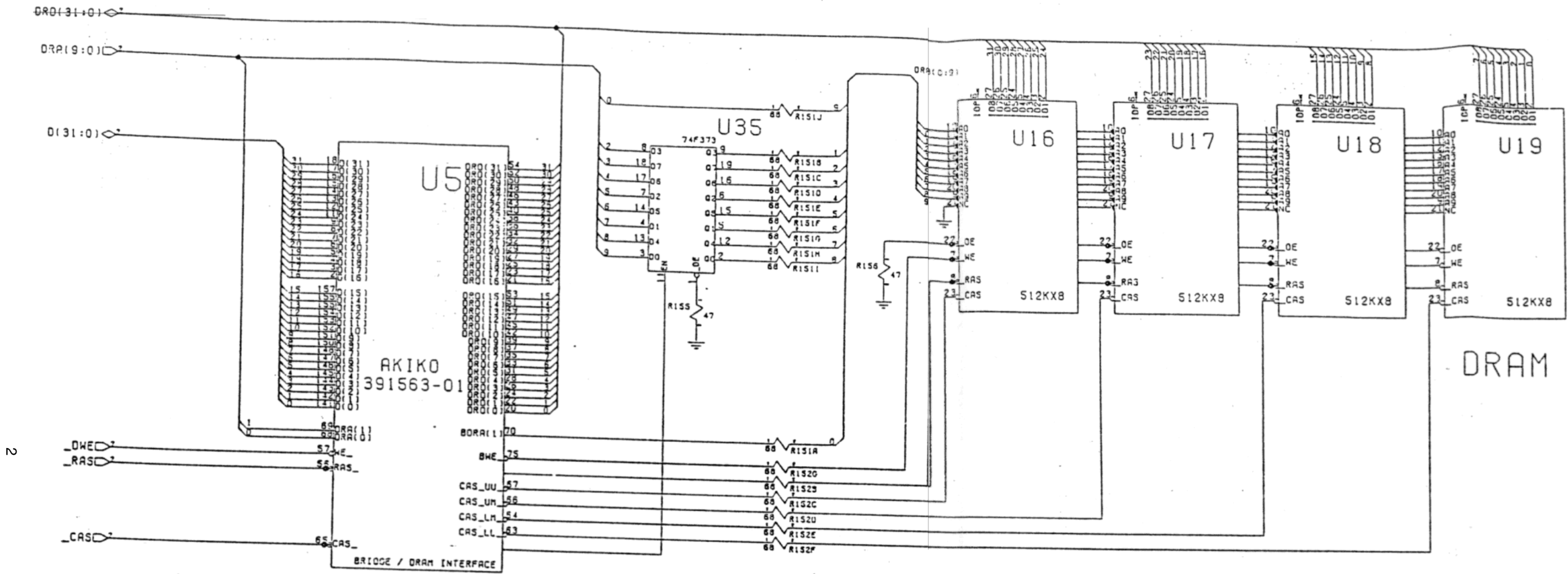
### KEY COMPONENTS

REF	CHIP	DESCRIPTION	PAGE
U1	68000	68000 PROCESSOR (16MHZ)	2
U2	8371	ALICE (RAM BUFFER)	2
U3	9361	PAULA	2
U4	1201	LESA (RAM DENISE)	2
U5	60228	RAM ARRAY (RAM ASIC)	2, 8, 11
U6	8551	RAM 512X16, 150 NS	10
U7-8	8520	RAM 512X16, 150 NS	10
U10-11	28F10	FLASH MEMORY (16K)	10
U12	74114	SQWAVE VIDEO ENCODER	1
U13	6570-3	ANALOG KEYBOARD MPU	9
U14	NE555	RESET TIMER	9
U15	LF347	BIPOLAR OP-AMP	9
U16	11004	BIPOLAR OP-AMP	ACT
U16-17	8551	URAM 256X16, 100 NS	3
U18-19	8551	URAM 256X16, OPTIONAL	3
U20	79177	ARITHMETIC INCR ASIC	3
U20	1490	LINE LINE DRIVER	7
U29	1490	LINE LINE RECEIVER	7
U30	01101	TRIPLE 0-011 VIDEO ORG	4
X1	05C	TTL 20.53636 MHZ MISC	2
	05C	TTL 20.53636 MHZ PAL	ACT
7451	X1AL	4.43619MHZ PAL BUFFER	4
7621	X1AL	36KHZ CLAMIC RESONATOR	9
X2	8551	PAL VIDEO MODULATOR	4
	8551	RISC VIDEO MODULATOR	4

REV 3, PCB

DIRECTORIES AND REVISION HISTORY

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W/GS PLAYER PCB

ROM DECOUPLING

32-BIT ROM OPTION

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MEMORY AND... WELL, I USED TO REMEMBER

COMODORE

SCHEMATIC CD/GB REV 3

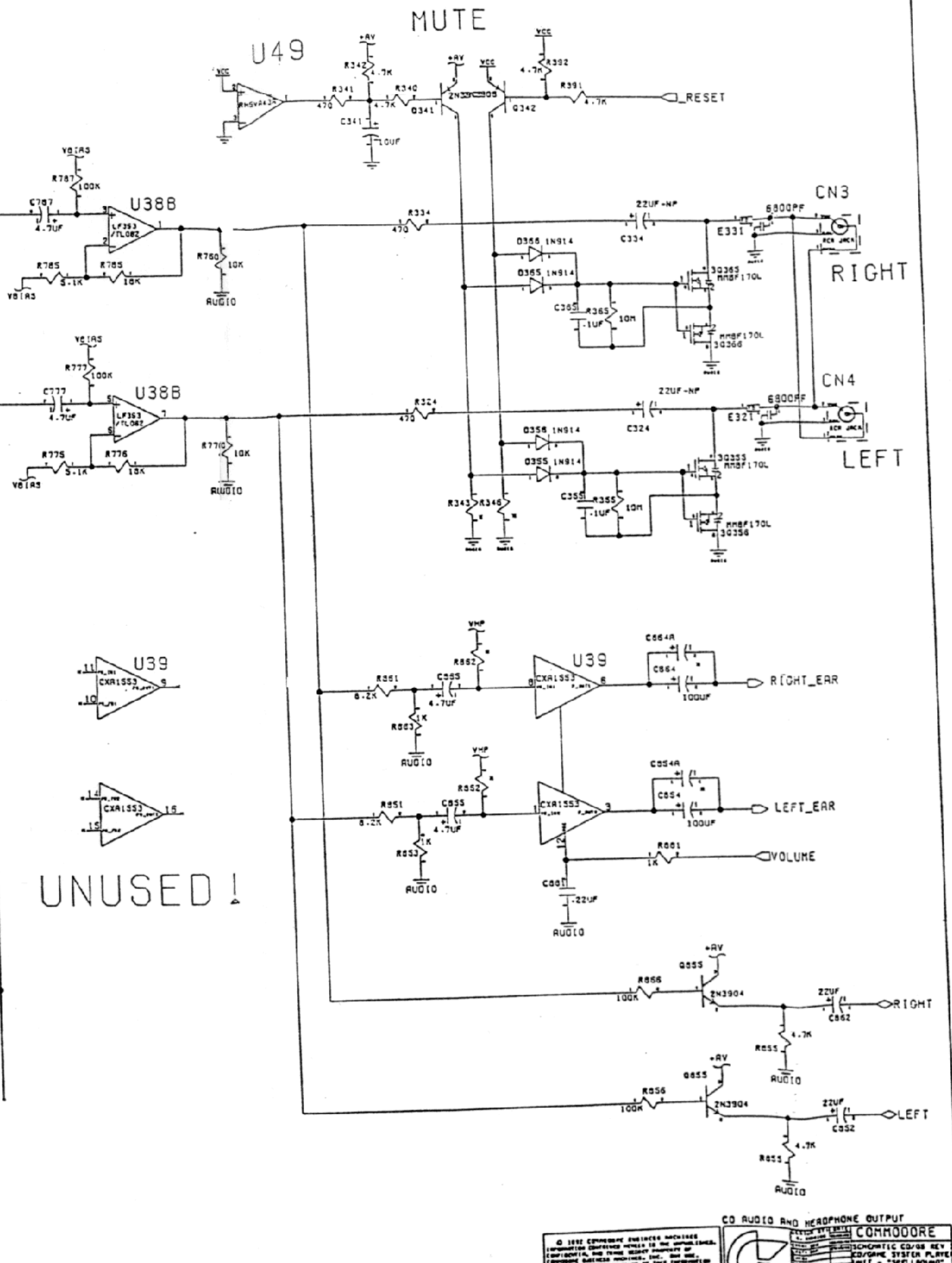
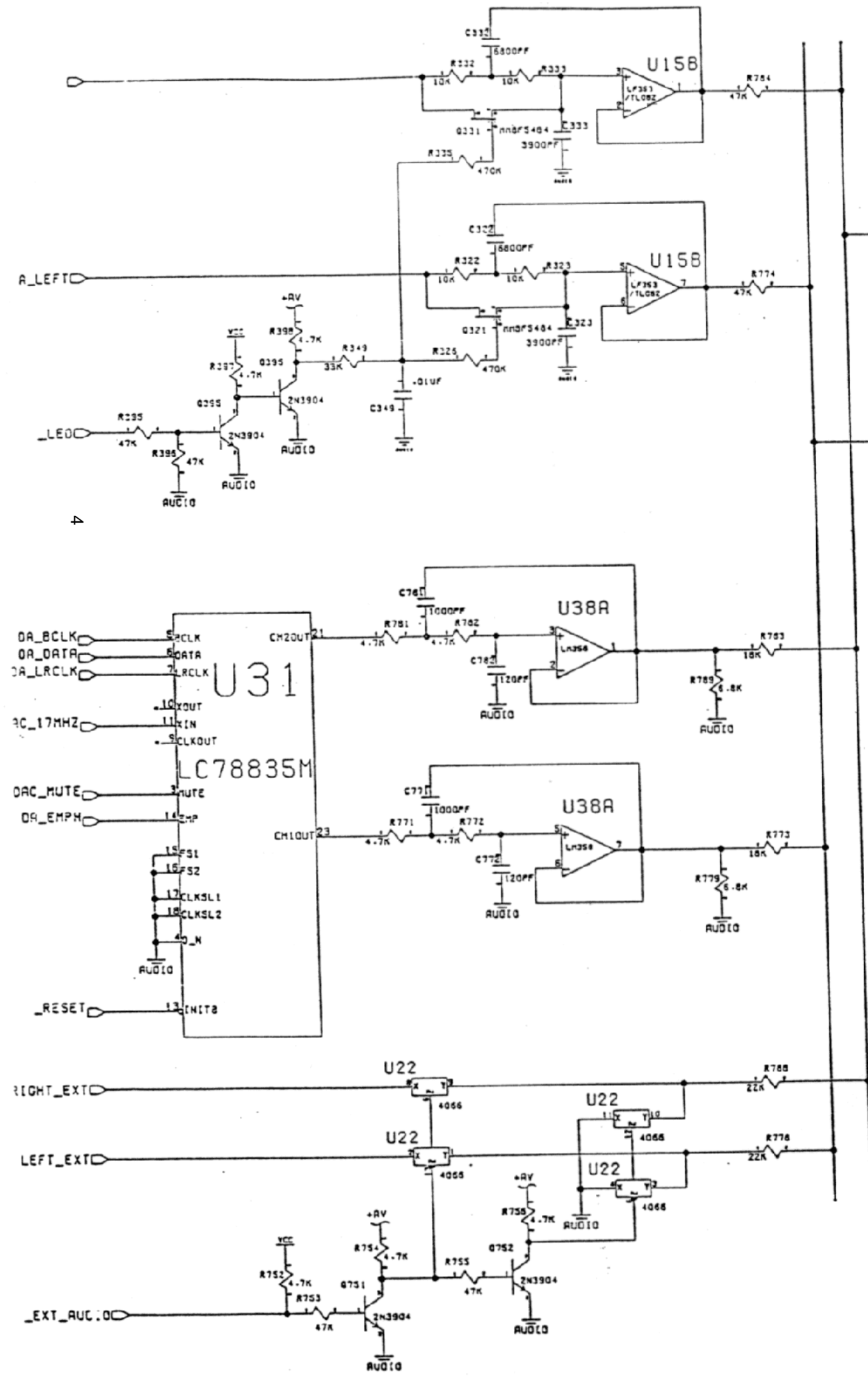
CD/GB SYSTEM PLAYER UNIT - "SPELLBOUND"

C.A.D. GENERATED

C1365100

SHEET 2 OF 10





CD/GS PLAYER PCB

CD AUDIO AND HEADPHONE OUTPUT

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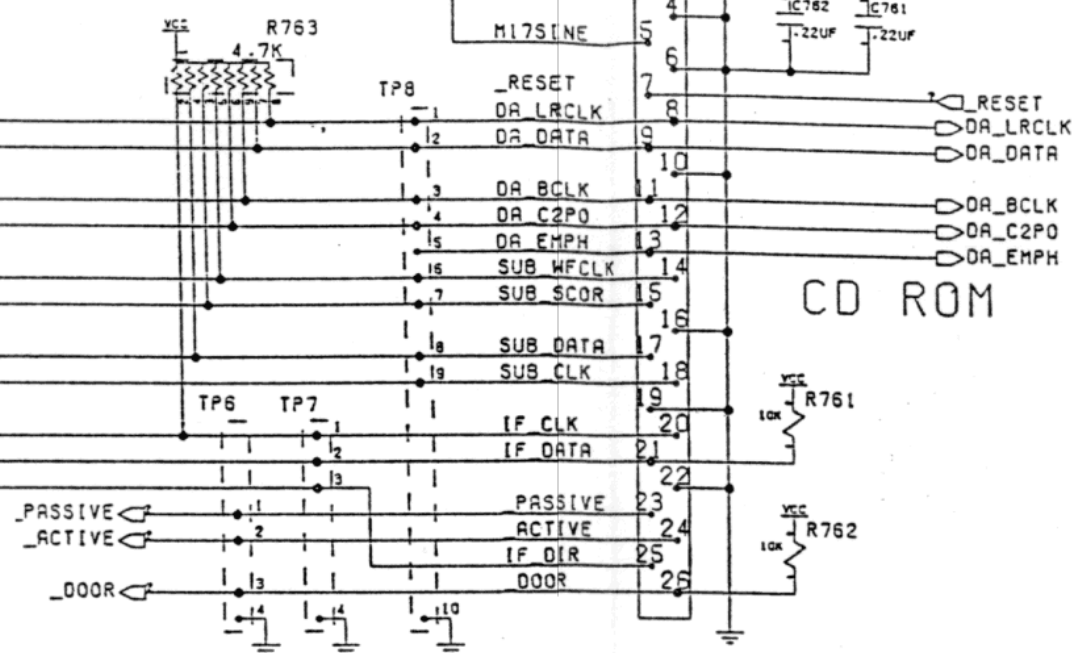
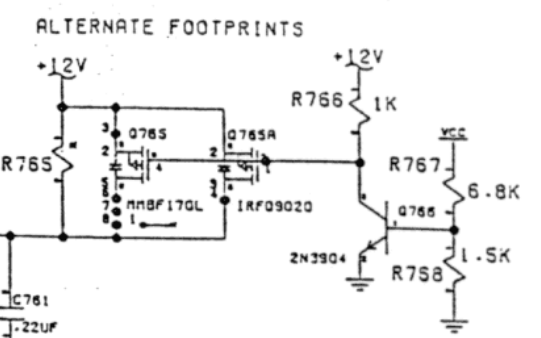
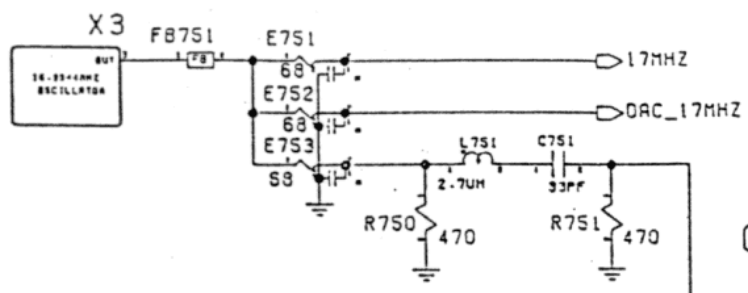
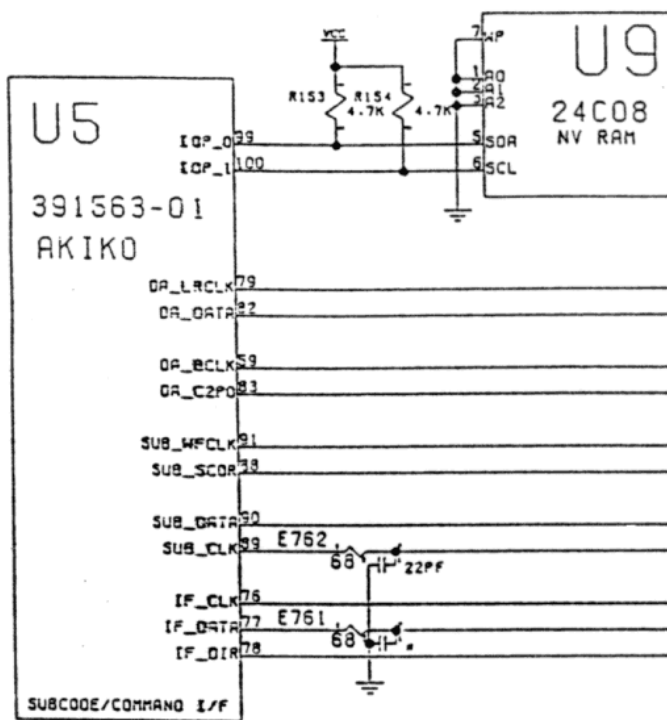
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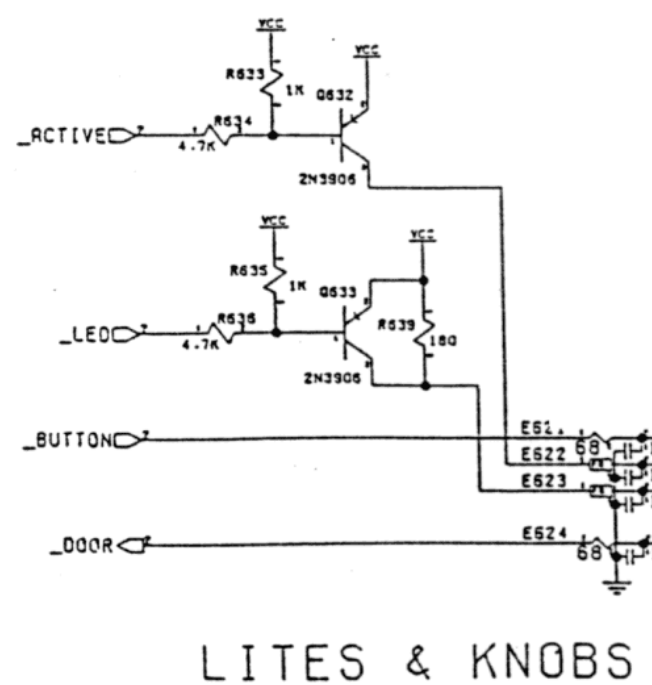
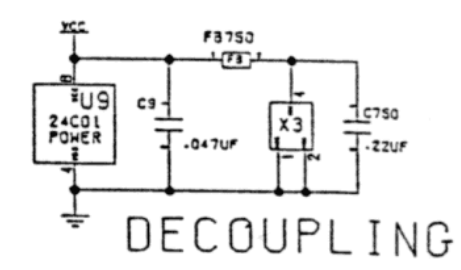
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REV: 1

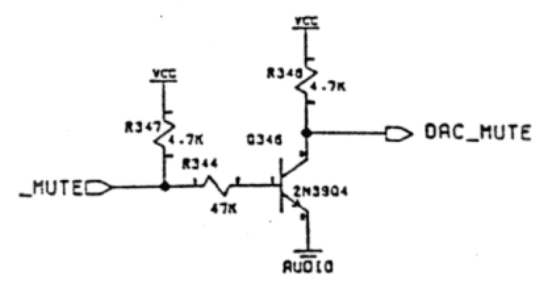
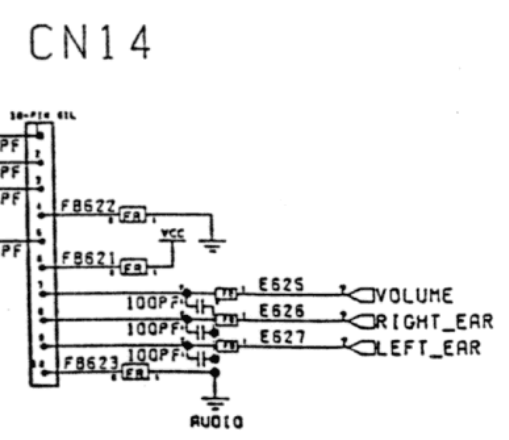
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25 PIN CD CONNECTOR

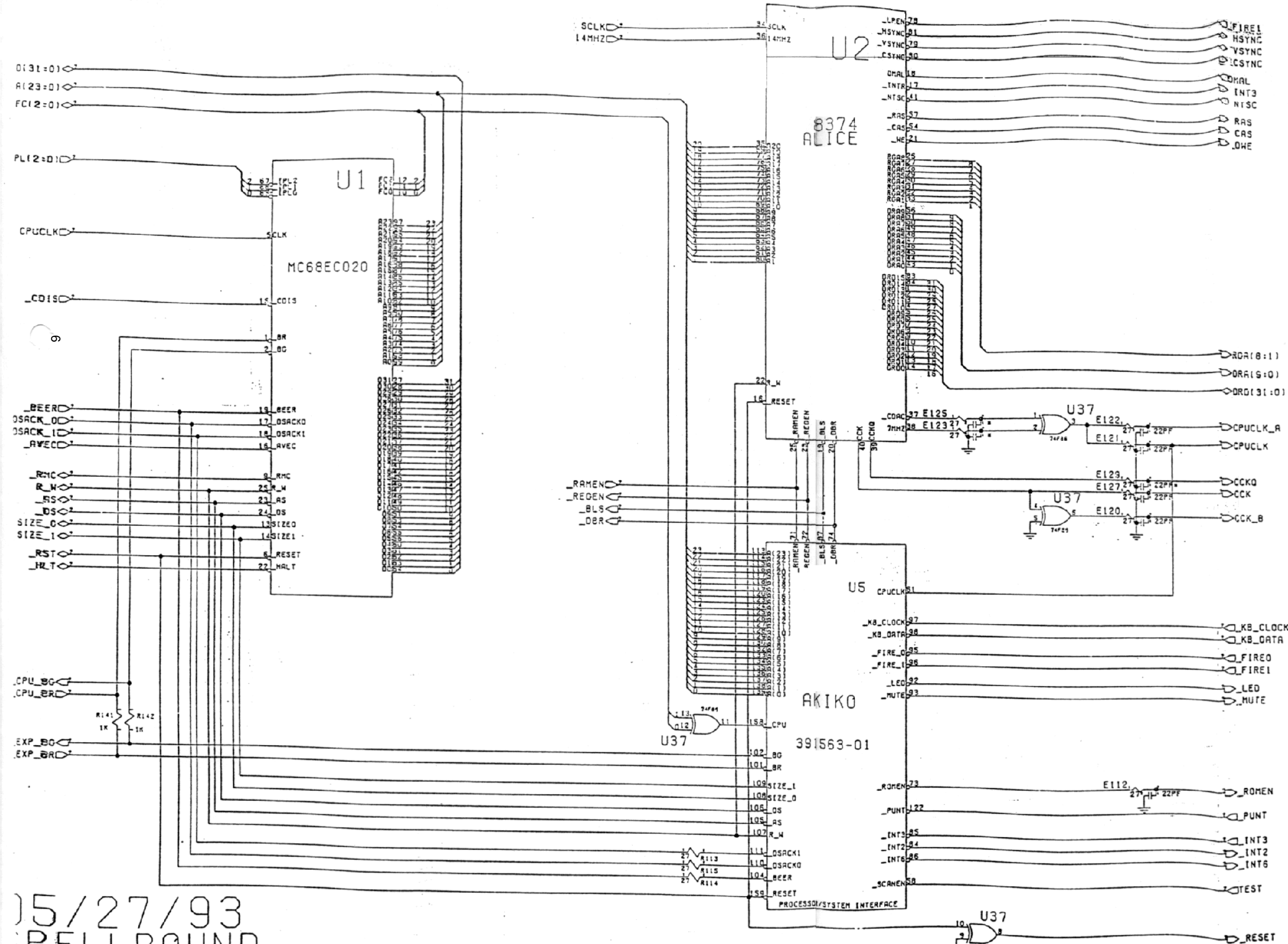


LITES & KNOBS



INVERTER





05/27/93  
 PELLBOUND  
 LOGS PLAYER PCB

NOTE: VARIOUS COMPONENTS ARE FOR EMI CONTROL  
 AND MAY BE LOADED WITH FUNNY THINGS...

PROCESSOR AND OTHER USEFUL COMPONENTS

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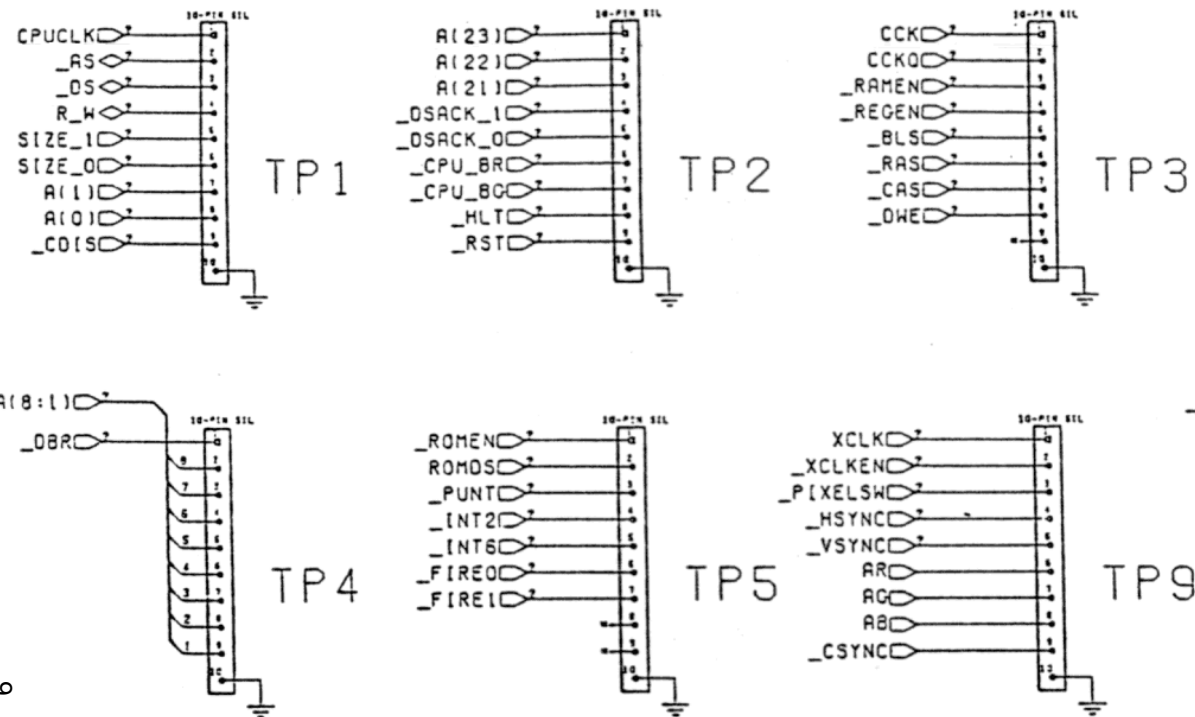
C.A.G. GENERATED

COMODORE  
 SCHEMATIC EDITOR REV 1  
 C64/C65 SYSTEM PLAYER  
 FILE - "SPELLBOUND"  
 C1365100  
 SHEET 2 OF 10



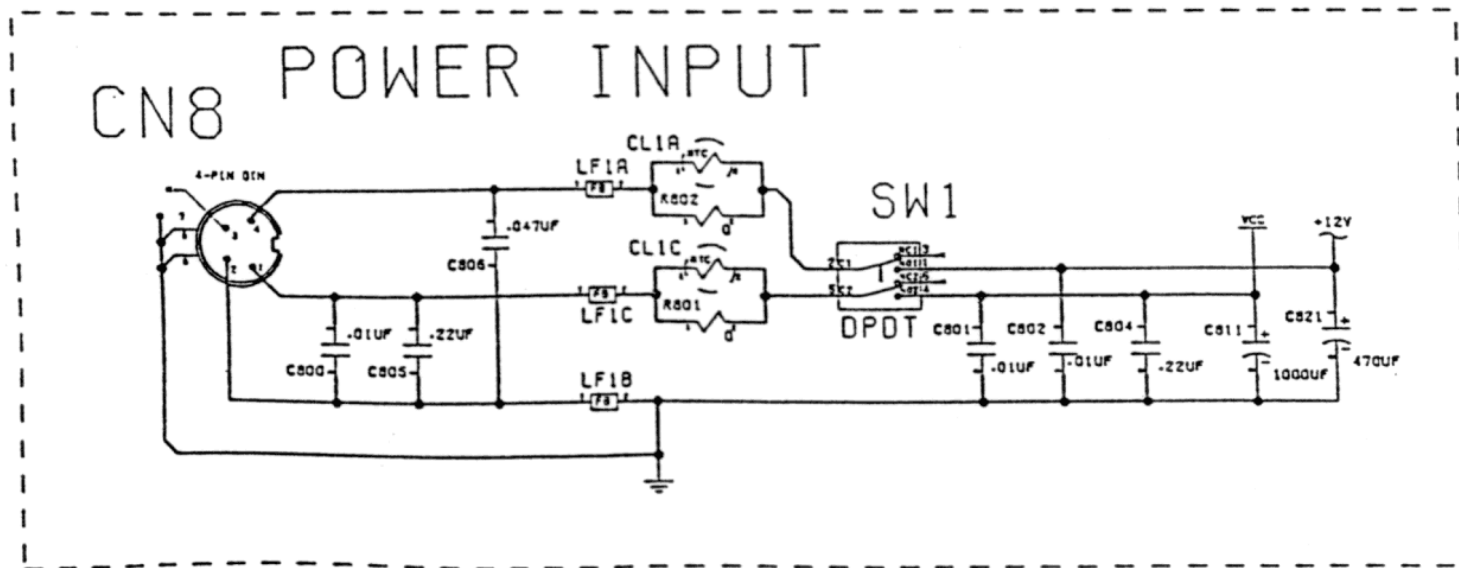
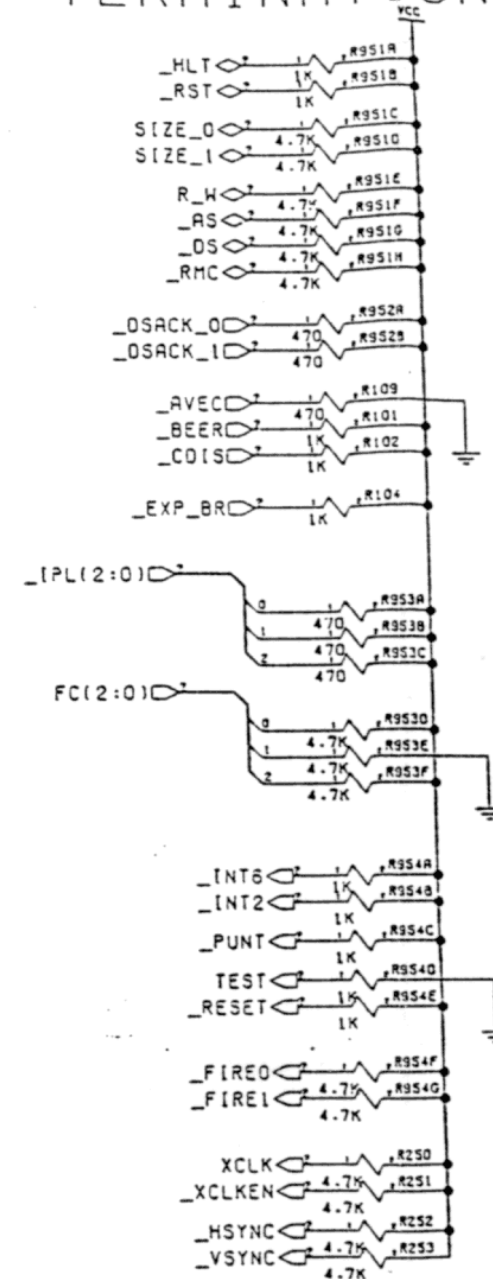






TEST ACCESS

TERMINATION



HOLES & C.

