Revision History

REV	DESCRIPTION	DATE	APRVL	MANAGER
0	Proof of Concept Prototype	4/29/91	GRR	

ECO Log

ECO NUMBER	DESCRIPTION	DATE

Jumpers and Stuff

REF	TYPE	DESCRIPTION	PAGE
JP1	BLOB	Keyboard Reset	7
JP2	BLOB	C0 vs. 08 Address Map	2
JP3	BLOB	Expansion RAS Select	3
JP4	BLOB	Bypass 2M-Byte Decoder	3
JP7	BLOB	Expansion/Tick Option	6
JP8	BLOB	Light Pen Port Select	6
JP9	BLOB	On-Board RTC Bypass	8
JP10	BLOB	RS232 Audio I/O Cutout	5
JP11	BLOB	TTL vs RS170 Comp Sync	4

Connectors

REF	TYPE	DESCRIPTION	PAGE
CN1	DB9P	Mouse/Joystick 1	2
CN2	DB9P	Mouse/Joystick 2	2
CN3	RCA-J	Right Audio Output	4
CN4	RCA-J	Left Audio Output	4
CN5	DD23S	External Floppy	7
CN6	DB25P	RS232 Serial Port	6
CN7	DB25S	Parallel Printer Port	6
CN8	SQ DIN	Power Supply Connector	8
CN9	DB23P	Video Output	5
CN10	RCA-J	Composite Video	5
CN11	DIL-34	Internal Floppy Signal	7
CN12	SIL-4	Internal Floppy Power	8
CN13	SIL-8	Keyboard Connector	6
P1	EDGE86	Expansion Connector	7
P9	RA-56H	Mem. Exp. Main-Board	8

Signal Glossary

SIGNAL	DESCRIPTION (AREA)	PAGES
28MHZ	28.63636 MHz Master Clock	2
7MHZ	7.15909 MHz Processor Clock	2,5
A[23:1]	Processor Address Bus (68000)	2,3,7
ACK	Data Acknowledge (Parallel Port)	6
AS	Address Strobe (68000)	2,7
AUDIN	Audio Input (RS232 Port)	4,6
AUDOUT	Audio Output (RS232 Jack)	4,6
BEER	Bus Error (68000)	2,7
BG	Bus Grant (68000)	2,7
BGACK	Bus Grant Acknowledge (68000)	2,7
BLISS	Blitter Slowdown (Chips)	2
BLIT	Chip Memory Access (Chips)	2,7
BR	Bus Request (68000)	2,7
BUSY	Device Busy (Parallel Port)	6
CASL/U	Column Address Strobe (DRAM)	2,3
CCK/CCKQ	Color Clock / Quadrature (Chips)	2,4,7
CDAC	7.15909 MHz Quadrature Clock (Chips)	2,5,7
CHNG	Media Change (Floppy)	6,7
CLKRD/WR	Read-Time Clock Read / Write (RTC)	2,9
COMP	Monochrome Composite Video (Video)	5
CSYNC	Composite Sync (Video)	2,5
CTS	Clear to Send (RS232 Port)	6
D[15:0]	Processor Data Bus (68000)	2,3,6,7
DIR	Step Direction (Floppy)	6,7
DKRD	Disk Read Data (Floppy)	4,7
DKWD	Disk Write Data (Floppy)	4,7
DKWE	Disk Write Enable (Floppy)	4,7
DMAL	Chip DMA Request Line (Chips)	2,4
DRA[8:0]	DRAM Address Bus (DRAM)	2,3
DRD[15:0]	DRAM Data Bus (DRAM)	2,3,4,5
DSR	Data Set Ready (RS232 Port)	6
DTACK	Data Transfer Acknowledge (68000)	2,3,7
DTR	Data Terminal Ready (RS232 Port)	6
E	Peripheral Enable Clock (68000)	2,6,7
EXTICK	Expansion Present / RTC Tick	2,3
FC[2:0]	Function Code (68000)	2,7
FIRE0/1	Fire Button 0/1 (Joysticks)	2,5,6
HLT	Processor Halt (68000)	2,7
HSYNC	Horizontal Sync (Video)	2,5,6
INDEX	Index Pulse (Floppy)	6,7
INT[2,3,6]	Interrupt Request (Chips)	2,4,6,7
IORESET	I/O Reset	6,7
IPL[2:0]	Interrupt Priority Level (68000)	2,4,7
KBCLOCK	Keyboard Clock (Keyboard)	6
KBDATA	Keyboard Data (Keyboard)	6
KBRESET	Keyboard Reset (Keyboard)	6
LDS/UDS	Upper / Lower Data Strobes (68000)	2,7
LED	Power On LED / Audio Filter Disable	4,6
LEFT/RIGHT	Left Right Audio (Audio)	4

SIGNAL	DESCRIPTION (AREA)	PAGES
LPEN	Light Pen Trigger (Joysticks)	2,6
MIR	Motor On (Floppy)	4,6
MIR0	Motor On - Drive 0 (Floppy)	4,6,7
M0V/M0H	Mouse 0 Quadrature V/H (Joysticks)	5
M1V/M1H	Mouse 1 Quadrature V/H (Joysticks)	5
OVL	Overlay ROM over RAM	2,6
OVR	Override System Decoding	2,7
PIXELSW	Genlock Pixel Switch (Video)	5
POT0X/0Y	Pot Lines 0 X/Y (Joysticks)	4,5
POT1X/1Y	Pot Lines 1 X/Y (Joysticks)	4,5
POUT	Paper Out (Parallel Port)	6
PPD[7:0]	Parallel Port Data (Parallel Port)	6
RAMEN	RAM Enable (Chips)	2
REGEN	Chip Register Enable (Chips)	2
RAS0/1	Row Address Strobe (DRAM)	2,3
RDY	Drive Ready (Floppy)	6,7
RESET	General Reset	6,7
RGA[8:1]	Register Address Bus (Chips)	2,4,5
R/G/B	Red / Green / Blue (Video)	5
RI	Ring Indicate (RS232 Port)	6
ROMEN	ROM Enable (ROM)	2,3
RTS	Request to Send (RS232 Port)	6
RST	Processor Reset (68000)	2,4,7
RXD	Receive Data (RS232 Port)	4,6
RW	Processor Read/Write (68000)	2,6,7
SEL	Select (Parallel Port)	6
SEL[3:0]	Drive Select (Floppy)	4,6,7
SIDE	Side Select (Floppy)	6,7
STEP	Step In/Out Command (Floppy)	6,7
TRK0	Track Zero Sense (Floppy)	6,7
TXD	Transmit Data (RS232 Port)	4,6
VMA	Valid Memory Address (68000)	2,6,7
VPA	Valid Peripheral Address (68000)	2,7
VSYNC	Vertical Sync (Video)	2,5,6
WE	Write Enable (DRAM)	2,3
WPROT	Write Protect Sense (Floppy)	6,7
XCLK	External Genlock Clock (Video)	2,5
XCLKEN	External Clock Enable (Video)	2,5
XRDY	External Data Ready	2,5

Key Components

REF	CHIP	DESCRIPTION	PAGE
U1	68000	68000 Processor, 8MHz	2
U2	8372	Agnus HR	2
	8371	Fat Agnus - PAL	alt
	8370	FAT Agnus - NTSC	alt
U3	8364	Paula	4
U4	8373	Denise HR	5
	8362	Denise	obs
U5	5719	Gary	2,4
U6	asst	ROM 128Kx16, 200 nS	3
U7-8	8520	Amiga VIA, 1 MHz	6
U14	LF347	BiMOS Op-Amp	4
	TL084	BiMOS Op-Amp	alt
U38	1488	EIA Line Driver	4
U39	1489	EIA Line Receiver	4
U42	NE555	Timer	7
U16-19	asst	DRAM 1Mx1, 120 nS	3
U20-23	asst	DRAM 1Mx1, 120 nS	9
X1	OSC	TTL 28.63636 MHz NTSC	2
	OSC	TTL 28.37512 MHz PAL	alt
HY1	asst	Video Hybrid	5

A300 Rev 0 PCB

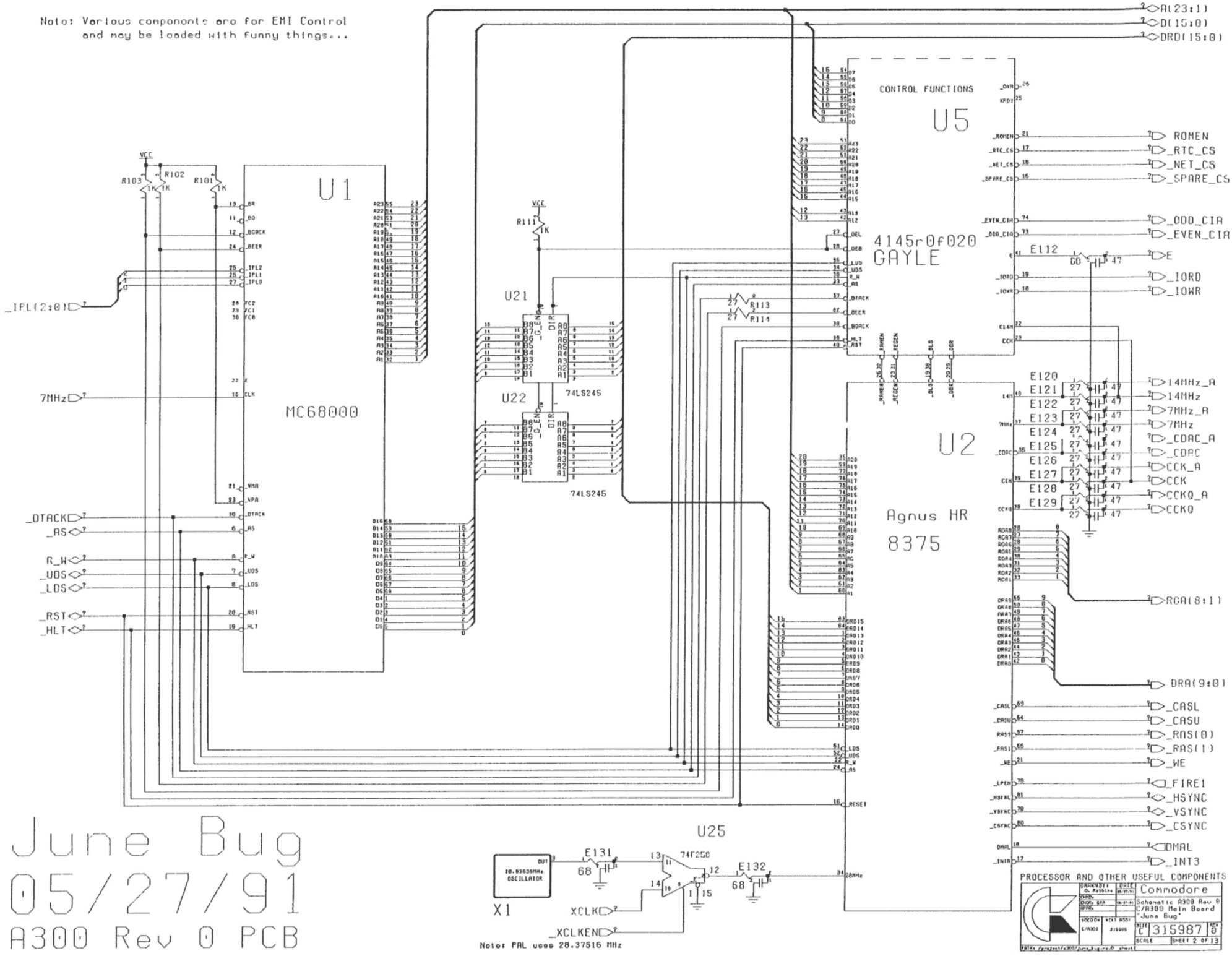
A PAGE FOR LARRY AND PERVEEN TO USE

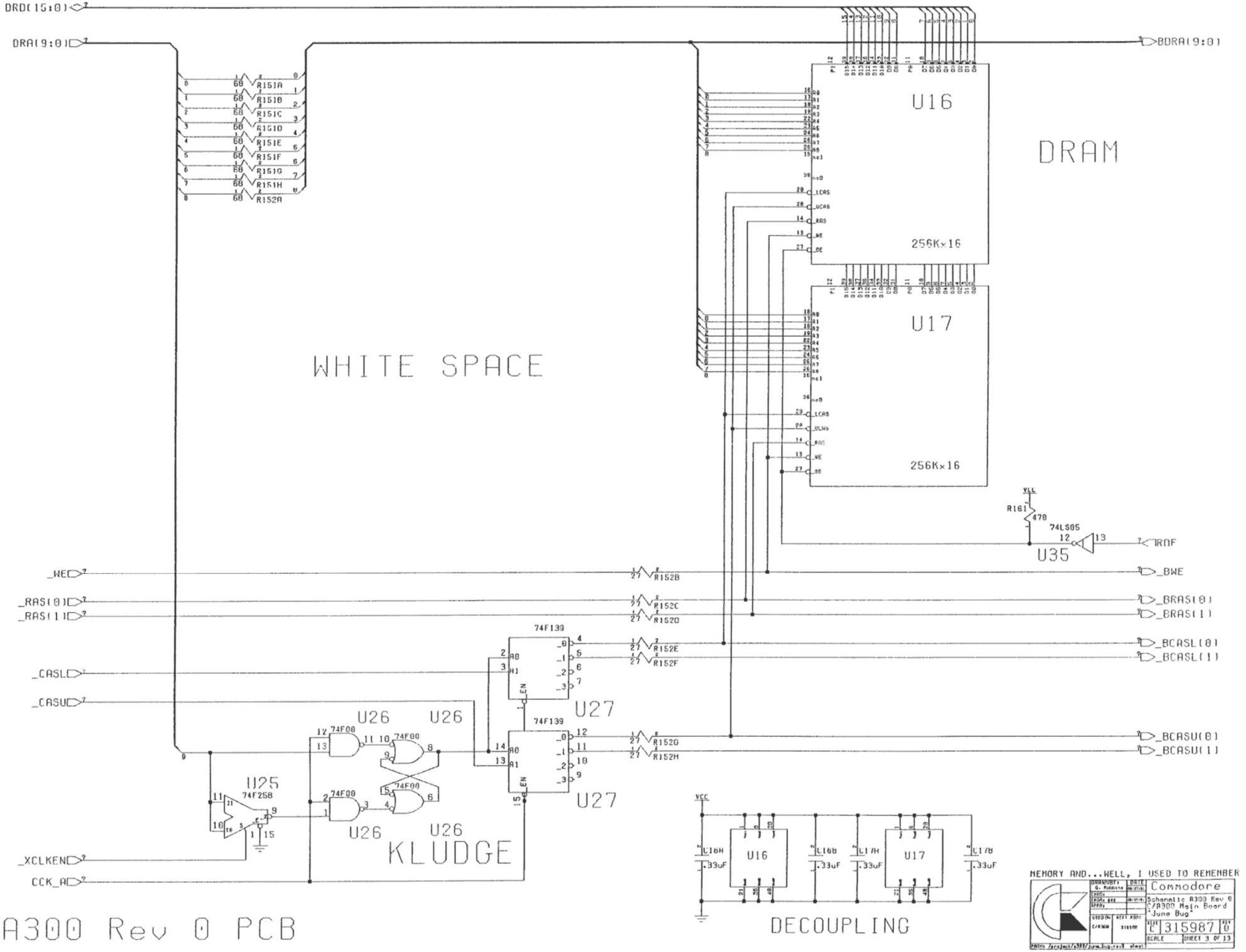
Commodore

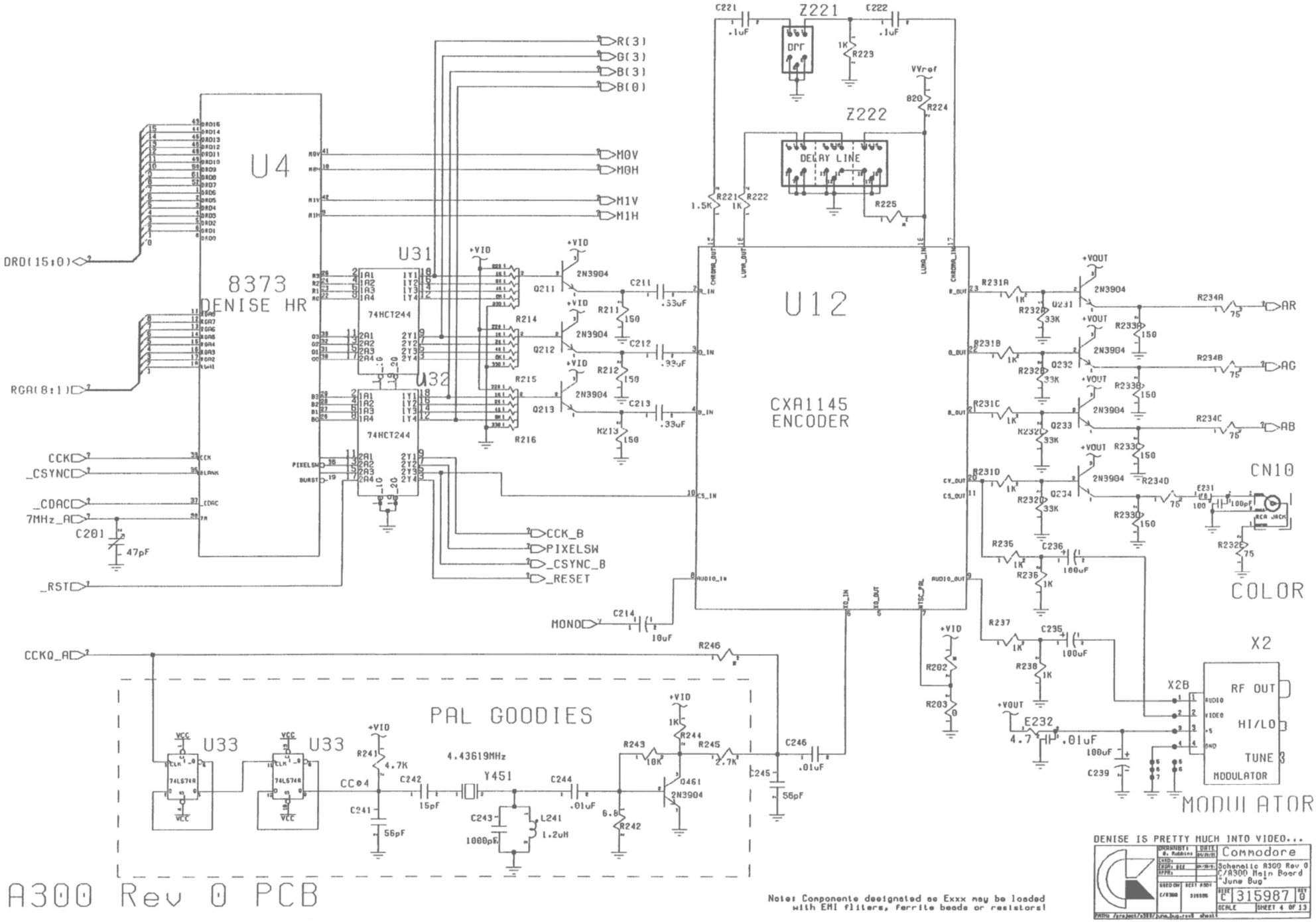
Domestic A300 Rev B
C/A300 Main Board
"June Bug"

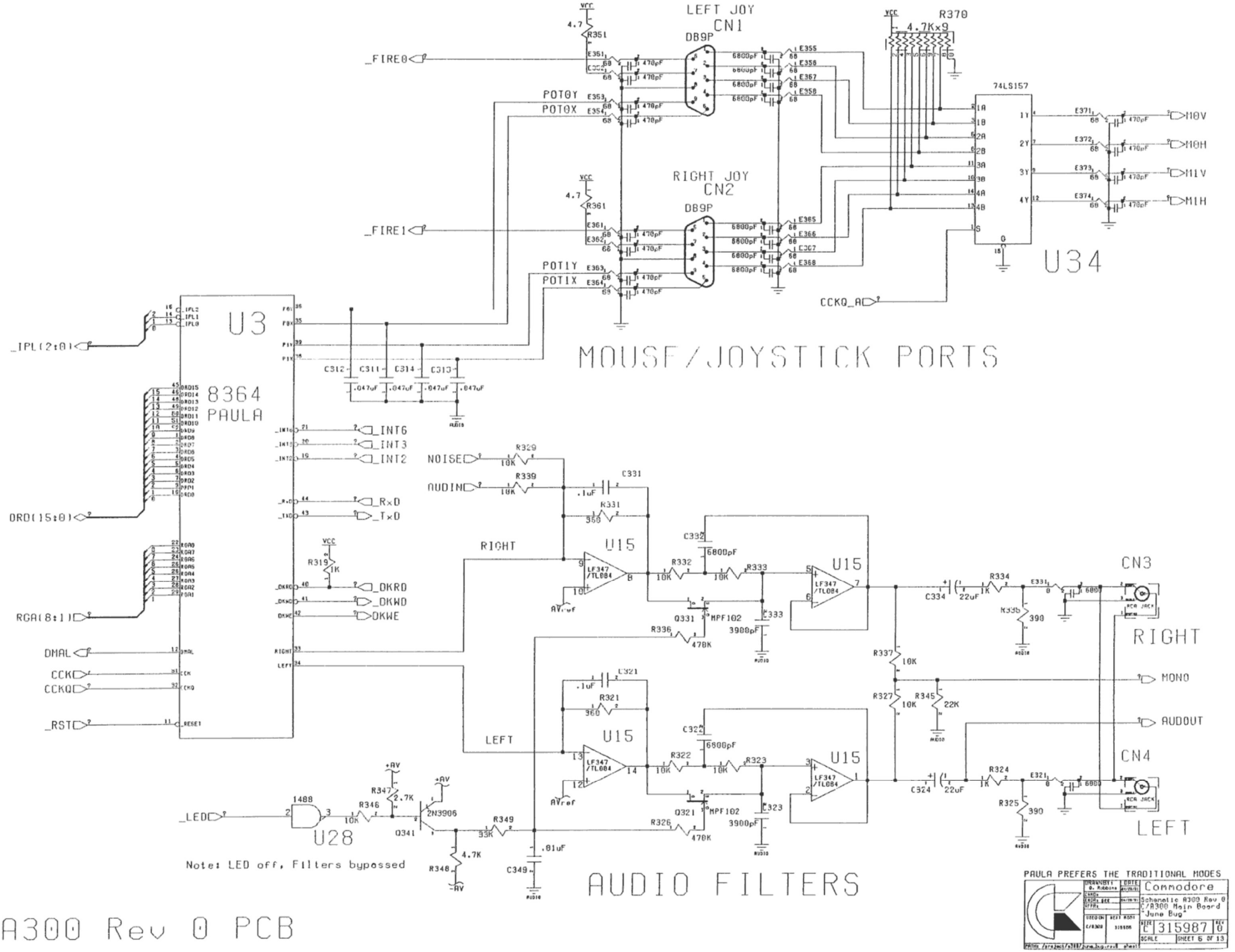
SIZE C | 315987 | REV 0

SCALE | SHEET 1 OF 13


Note: Various componants are for EMI Control
and may be loaded with funny things...
A[23:1]
D[15:0]
DRD[15:0]
U1
MC68000
U5
CONTROL FUNCTIONS
4145r0f020
GAYLE
U2
Agnus HR
8375
U21
74LS245
U22
74LS245
U25
X1
28.63636MHz
OSCILLATOR
Note: PAL uses 28.37516 MHz
ROMEN
_RTC_CS
_NET_CS
_SPARE_CS
_ODD_CIA
_EVEN_CIA
E
_IORD
_IOWR
14MHz_A
14MHz
7MHz_A
7MHz
_CDAC_A
_CDAC
CCK_A
CCK
CCKQ_A
CCKQ
RGA[8:1]
DRA[9:0]
_CASL
_CASU
_RAS(0)
_RAS(1)
_WE
_FIRE1
_HSYNC
_VSYNC
_CSYNC
_DMAL
_INT3
_IPL[2:0]
7MHz
_DTACK
_AS
R_W
_UDS
_LDS
_RST
_HLT
VCC
R101
R102
R103
R111
R113
R114
1K
27
E112
E120
E121
E122
E123
E124
E125
E126
E127
E128
E129
47
E131
E132
68
74F250
PROCESSOR AND OTHER USEFUL COMPONENTS
Commodore
Schematic A300 Rev 0
C/A300 Main Board
"June Bug"
315987
SHEET 2 OF 13
June Bug
05/27/91
A300 Rev 0 PCB

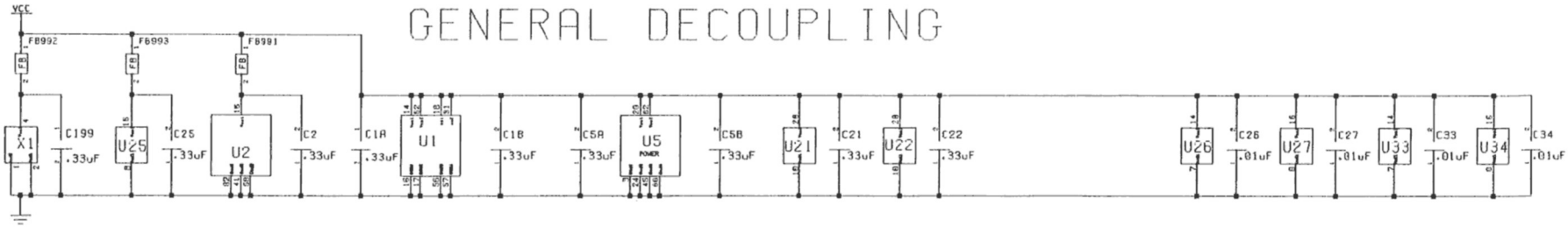

DRD[15:0]
DRA[9:0]
BDRA[9:0]
R151A
R151B
R151C
R151D
R151E
R151F
R151G
R151H
R152A
U16
DRAM
256K×16
U17
256K×16
WHITE SPACE
R161
470
74LS05
U35
IRNF
_WE
R152B
_BWE
_RAS[0]
_RAS[1]
R152C
R152D
_BRAS[0]
_BRAS[1]
74F139
U27
R152E
R152F
_BCASL[0]
_BCASL[1]
_CASL
_CASU
U26
74F00
U25
74F258
R152G
R152H
_BCASU[0]
_BCASU[1]
KLUDGE
_XCLKEN
CCK_A
VCC
C16A
C16B
C17A
C17B
.33uF
DECOUPLING
MEMORY AND...WELL, I USED TO REMEMBER
Commodore
Schematic A300 Rev 0
C/A300 Main Board
"June Bug"
315987
SHEET 3 OF 13
A300 Rev 0 PCB


U4
8373
DENISE HR
U31
U32
74HCT244
U12
CXA1145
ENCODER
Z221
Z222
DELAY LINE
DRD(15:0)
RGA(8:1)
CCK
_CSYNC
_CDAC
7MHz_A
C201
47pF
_RST
R(3)
G(3)
B(3)
B(0)
MOV
MOH
M1V
M1H
+VID
+VOUT
VVref
2N3904
CCK_B
PIXELSW
_CSYNC_B
_RESET
MONO
C214
10uF
CCKQ_A
R246
PAL GOODIES
U33
74LS74R
4.43619MHz
Y451
CC04
C241
56pF
C242
15pF
C243
1000pF
L241
1.2uH
C244
.01uF
C245
56pF
C246
.01uF
R241
4.7K
R242
6.8
R243
10K
R244
1K
R245
2.7K
Q461
2N3904
R202
R203
0
X2
X2B
RF OUT
HI/LO
TUNE
MODULATOR
E232
4.7
.01uF
100uF
C239
CN10
RCA JACK
COLOR
AR
AG
AB
A300 Rev 0 PCB
DENISE IS PRETTY MUCH INTO VIDEO...
Commodore
Schematic A300 Rev 0
2/A300 Main Board
"June Bug"
SIZE C 315987 REV 0
SCALE
SHEET 4 OF 13
Note: Components designated as Exxx may be loaded with EMI filters, ferrite beads or resistors!

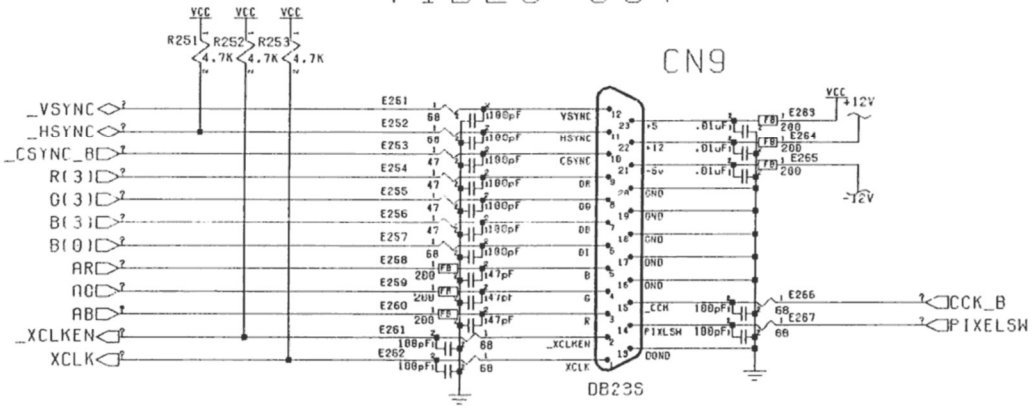


A300 Rev 0 PCB

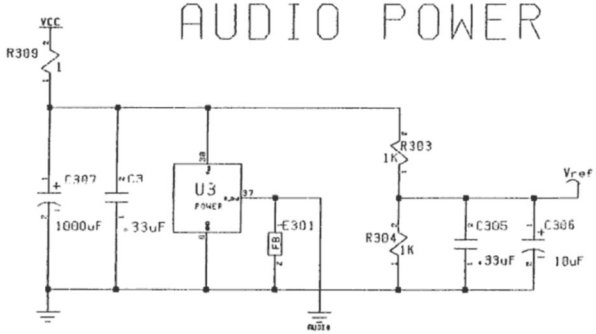
GENERAL DECOUPLING



VIDEO OUT

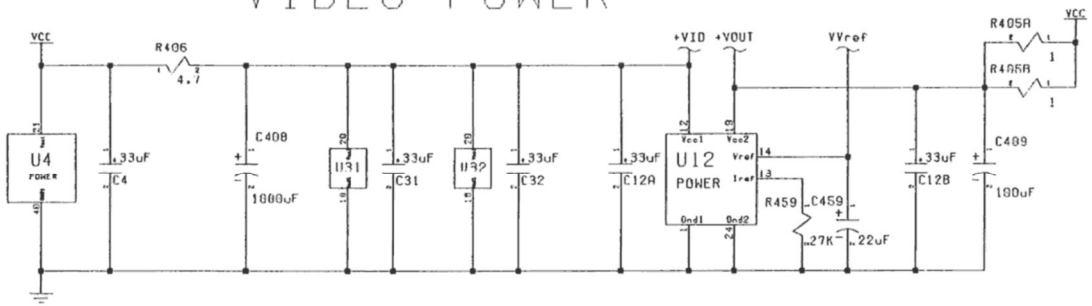


AUDIO POWER

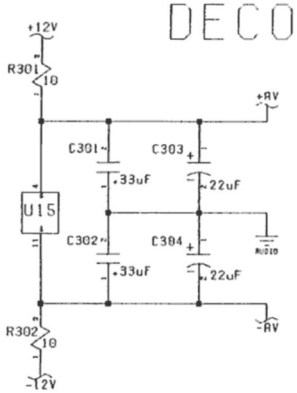


Note: Ground interconnection near audio jacks.

VIDEO POWER



DECOUPLING

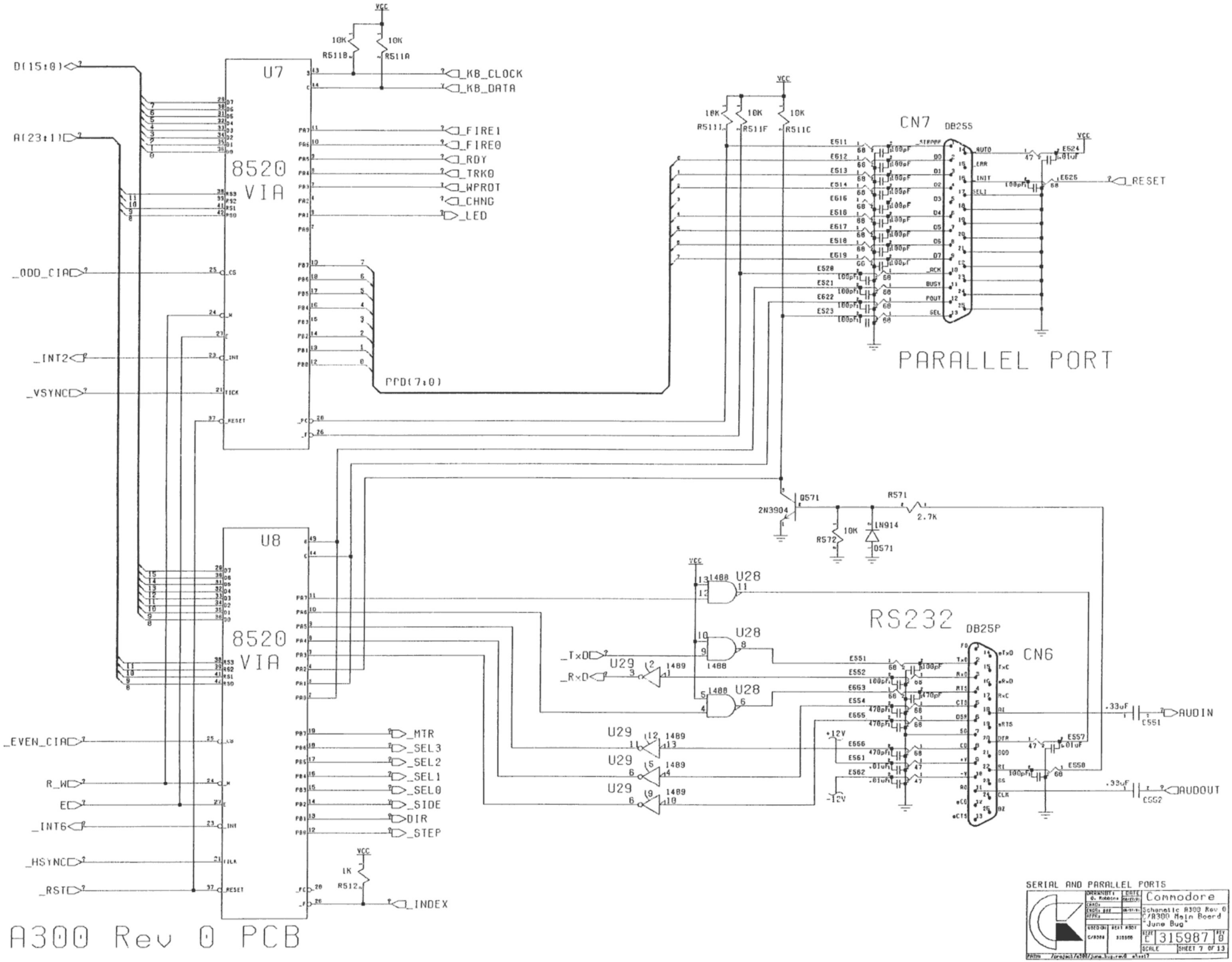


PARTY OUT OF BOUNDS, WHAT A MESS...

DRAWN/DATE	G. Robbins	06/28/91	Commodore
CHKD:			Schematic A300 Rev 0 C/A300 Main Board "June Bug"
ENGR: REV		06/28/91	
APPR:			
MFG DWG	C/A300	NEXT ASSY 315595	SIZE C 315987 REV 0
			SCALE SHEET 6 OF 13

PATH: /project/a300/june_bug.rev0 sheet6

A300 Rev 0 PCB



SERIAL AND PARALLEL PORTS

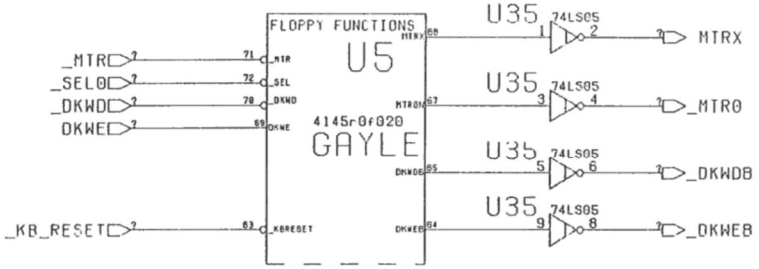
Commodore

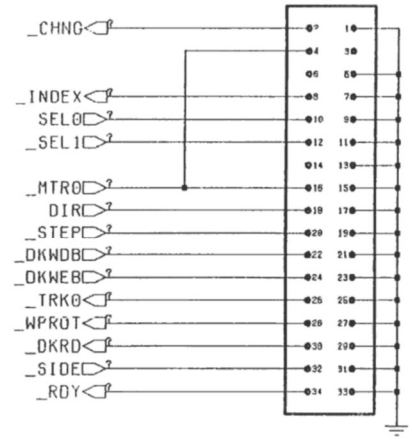
Schematic A300 Rev 0
C/A300 Main Board
"June Bug"

SIZE C | 315987 | REV 0

SCALE | SHEET 7 OF 13

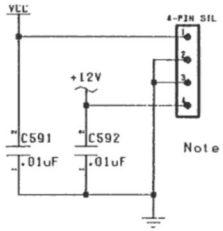
FLOPPY LOGIC





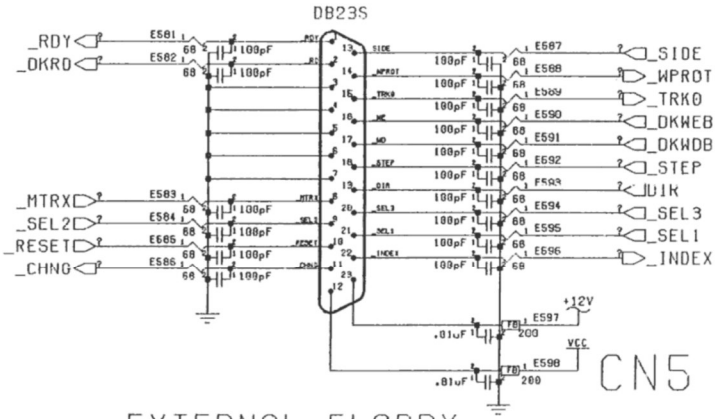
INTERNAL FLOPPY CN11

FLOPPY POWER



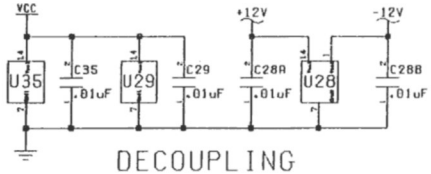
CN12

Note: Some drives are +5 only...



CN5

EXTERNAL FLOPPY



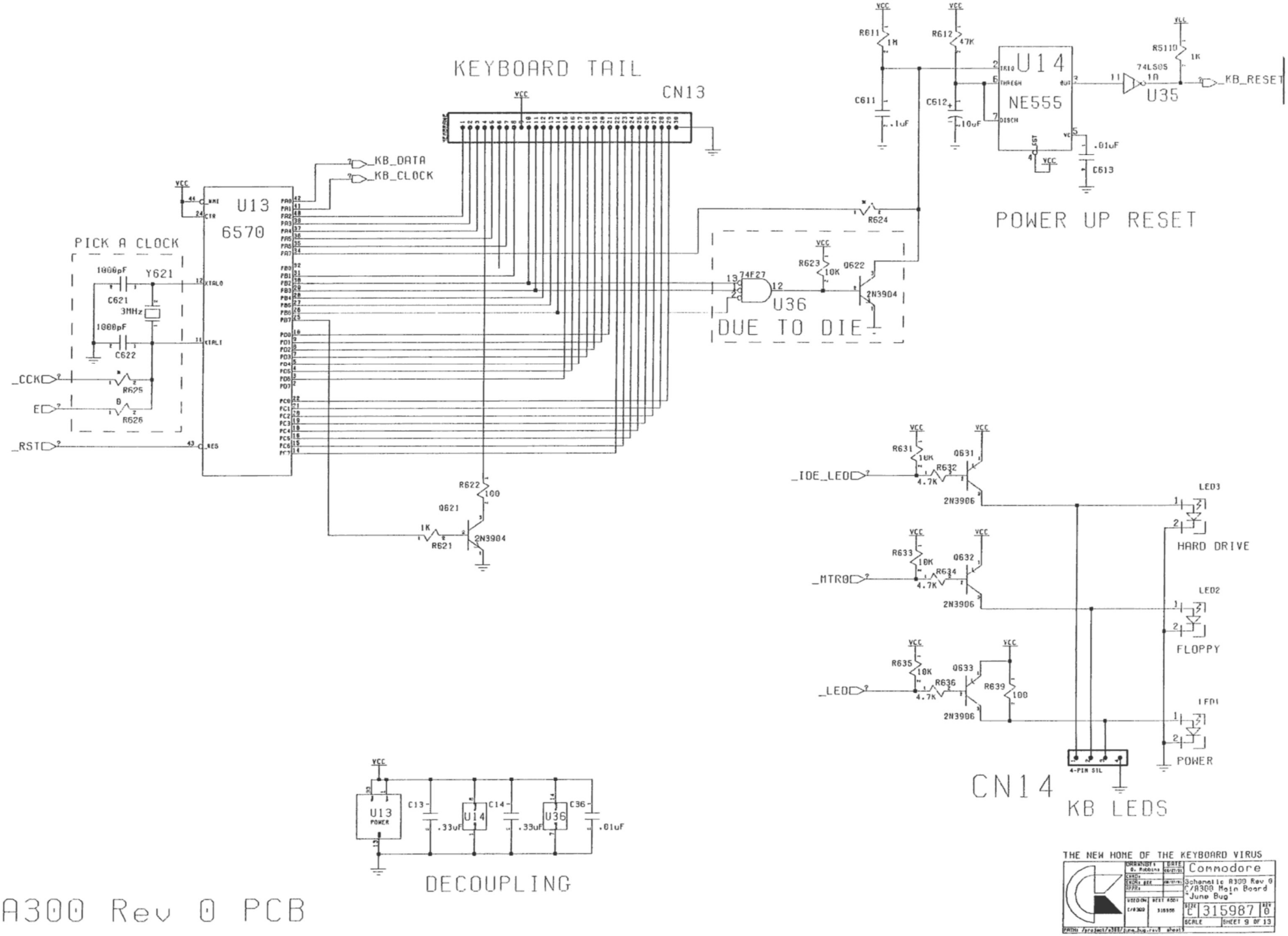
DECOUPLING

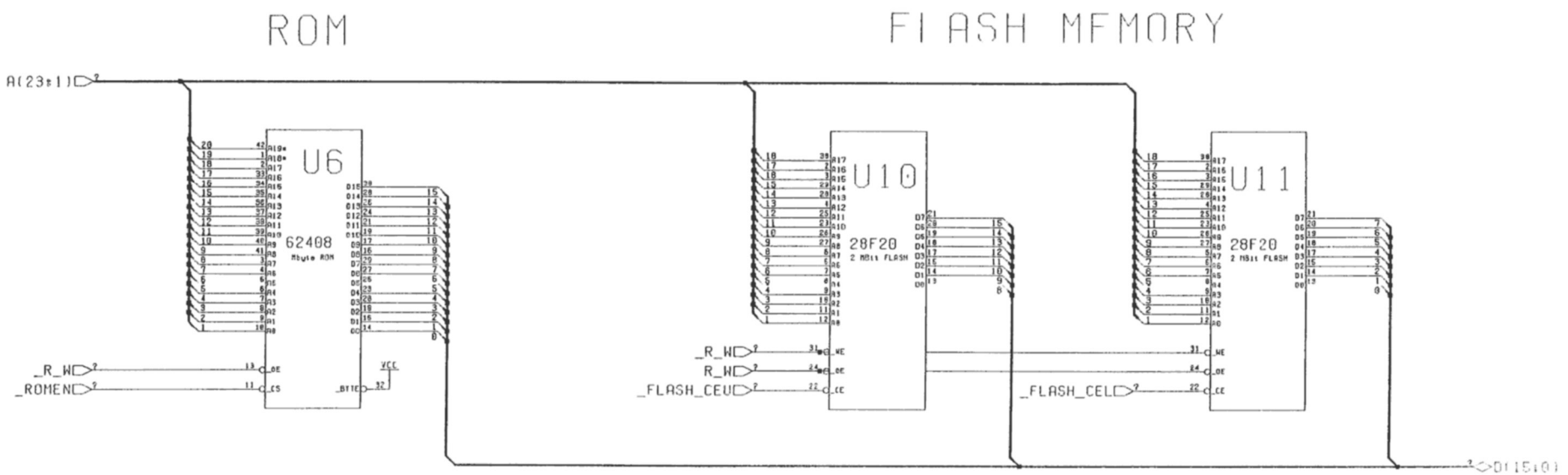
A300 Rev 0 PCB

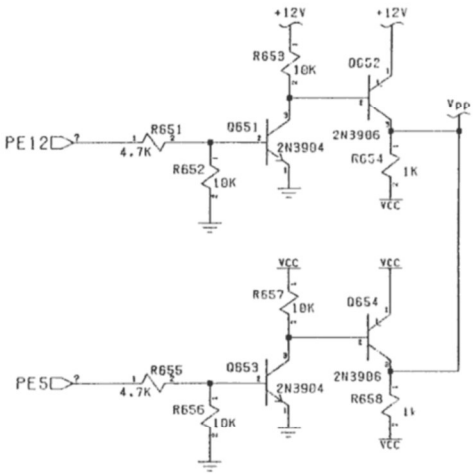
THE REST OF THE FLOPPY STUFF

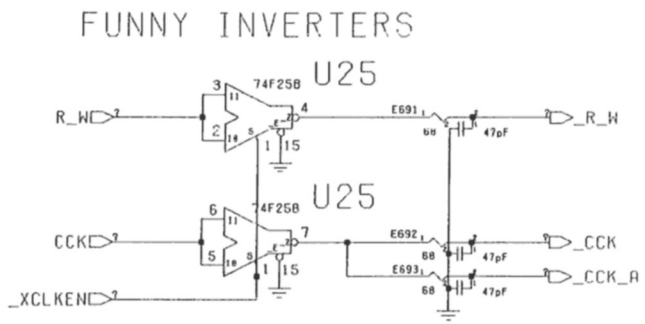
DRAWN BY: D. Robbins	DATE: 03-17-91	Commodore	
CHKD:		Schematic A300 Rev 0	
ENGR: REV	03-17-91	C/A300 Main Board	
APPR:		"June Bug"	
SIZE C	315987	REV 0	
SCALE		SHEET 8 OF 13	

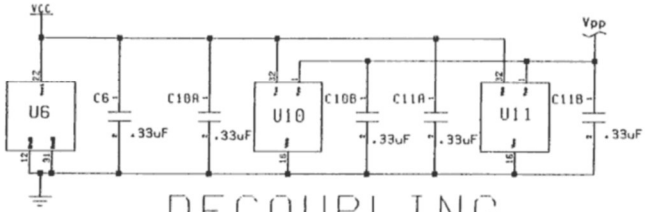
PATH: /project/a300/june_bug.rev0 sheet8


KEYBOARD TAIL
CN13
KB_DATA
KB_CLOCK
U13
6570
PICK A CLOCK
Y621
3MHz
C621
C622
1000pF
_CCK
E
_RST
R625
R626
R624
U14
NE555
R611
1M
R612
47K
C611
.1uF
C612
10uF
.01uF
C613
R5110
1K
74LS05
U35
KB_RESET
POWER UP RESET
U36
74F27
R623
10K
Q622
2N3904
DUE TO DIE
R622
100
Q621
1K
R621
2N3904
_IDE_LED
R631
10K
Q631
R632
4.7K
2N3906
LED3
HARD DRIVE
_MTR0
R633
10K
Q632
R634
4.7K
2N3906
LED2
FLOPPY
_LED
R635
10K
Q633
R636
4.7K
R639
100
2N3906
LED1
POWER
4-PIN SIL
CN14
KB LEDS
U13
POWER
C13
.33uF
C14
.33uF
C36
.01uF
DECOUPLING
A300 Rev 0 PCB
THE NEW HOME OF THE KEYBOARD VIRUS
Commodore
Schematic A300 Rev 0
C/A300 Main Board
"June Bug"
C 315987 0
SHEET 9 OF 13







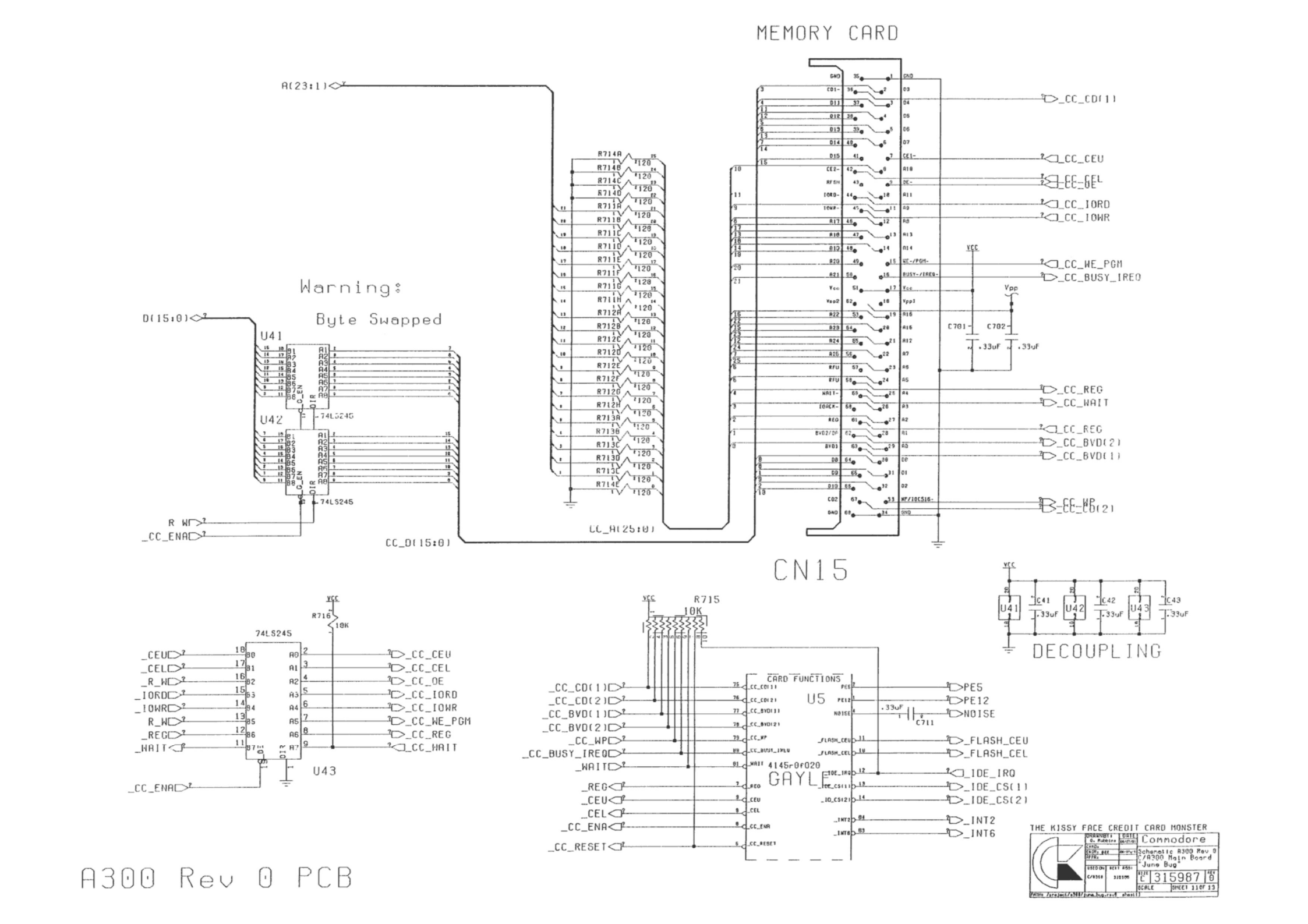


A300 Rev 0 PCB

ROM - PLAIN AND FANCY - DODADS TOO!

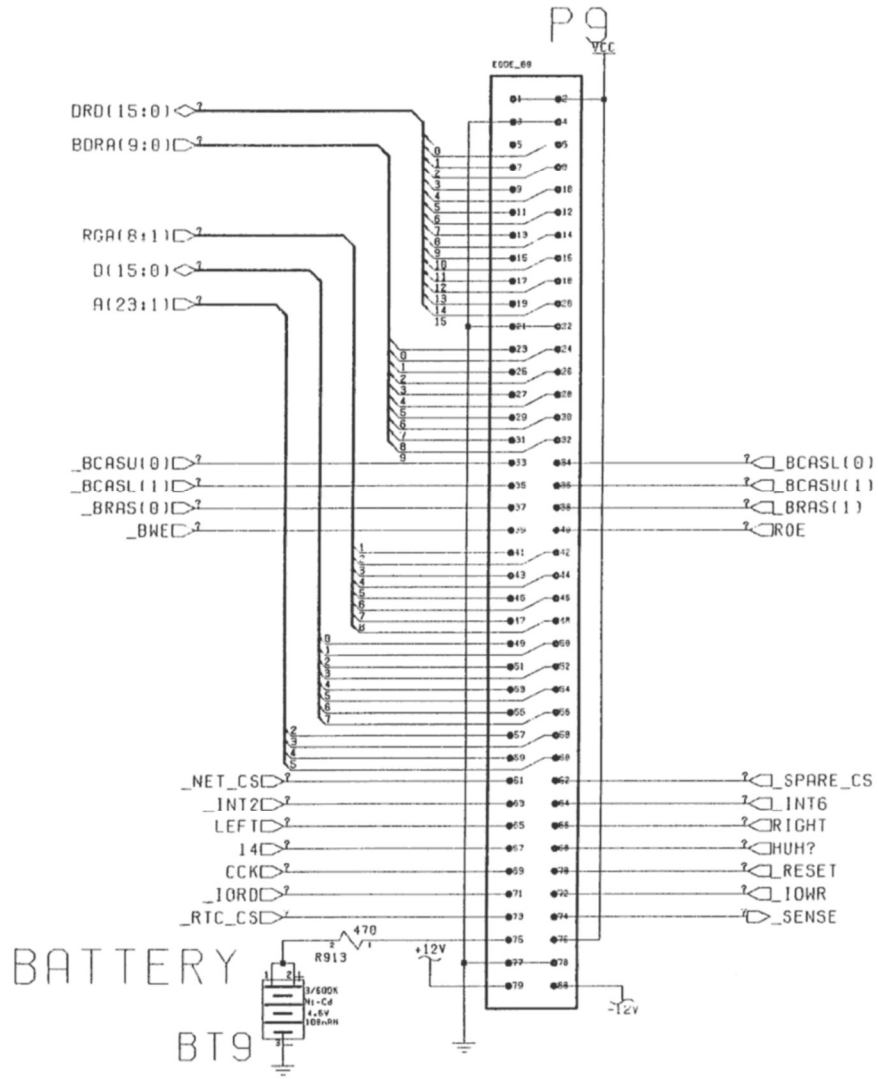
DRAWN BY: B. Robbins	DATE: 08/11/93	Commodore	
CHKD:			
ENGR: BEE	08/17/93	Schematic A300 Rev 0 2/A300 Main Board "June Bug"	
APPR:			
CURRENT: BEE1 A501			
C/A300	315985	SIZE: E	315987 REV: 0
		SCALE	SHEET 10 OF 13

PATH: /project/a300/june_bug.rev0 sheet10

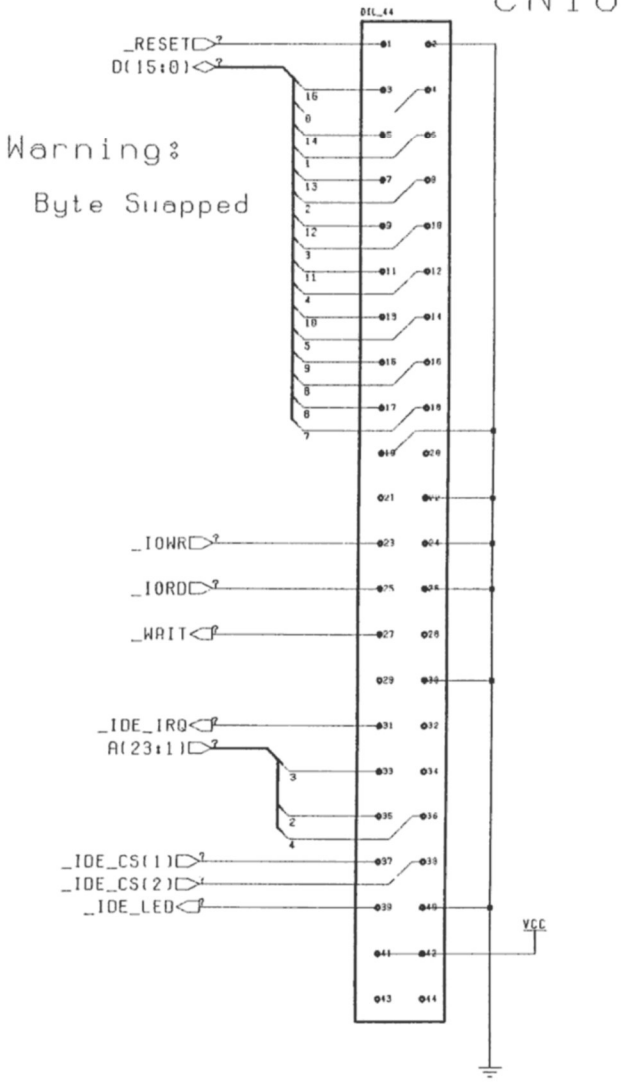


A300 Rev 0 PCB

MEMORY EXPANSION



IDE DRIVE



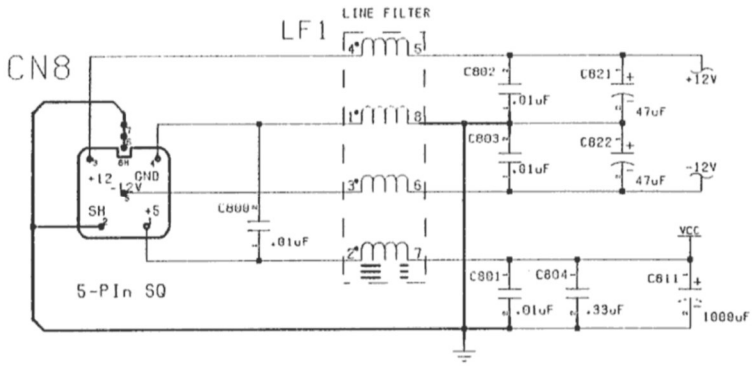
MEMORY EXPANSION AND THE IDE DRIVE

DRAWN/BY: G. Robbins	DATE: 06/17/91	Commodore	
CHKD:		Schematic A300 Rev 0 C/A300 Main Board "June Bug"	
ENGR: BEE	06/17/91		
APPR:			
SYSTEM: C/A300	NEXT ASSY: 315988	SIZE: C	315987 REV: 0
		SCALE	SHEET 12 OF 13

PATH: /project/a300/june_bug.revA sheet12

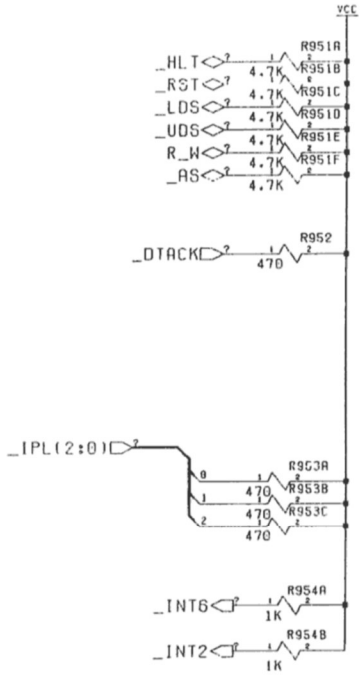
A300 Rev 0 PCB

POWER INPUT

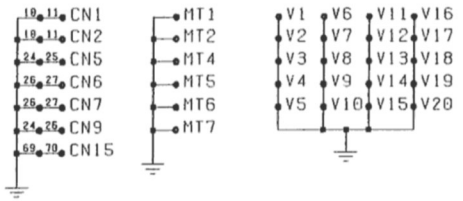


NOTE: HEAVY LINES INDICATE A SINGLE POINT CONNECTION

"BUS" TERMINATION



GROUNDED HOLES, &c.



A300 Rev 0 PCB

POWER DISTRIBUTION AND DECOUPLING

Commodore

Schematic A300 Rev 0
C/A300 Main Board
"June Bug"

SIZE C | 315987 | REV 0

SCALE

SHEET 13 OF 19